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A Digital Discrete-Time Non-Foster Approach to Broadband Fast-Wave Microstrip Lines

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***Abstract* – The design of a fast-wave microstrip line is presented, where analog negative capacitance circuits are replaced by digital discrete-time non-Foster circuits. Building upon recent results for a wideband three-section fast-wave microstrip line using three negative capacitors, the proposed digital approach is shown to exhibit fast-wave characteristics over wide bandwidth with phase velocity greater than the speed of light in vacuum. Quality factor of negative capacitors is known to limit bandwidth of analog non-Foster fast-wave lines, and similar behavior is observed in the digital non-Foster simulations. Nevertheless, the proposed digital non-Foster approach is shown to offer broadband fast-wave performance, even with limited quality factor.**

I. Introduction

Digital discrete-time implementations have been proposed for a number of non-Foster circuit elements such as negative capacitors and negative inductors [1–3]. This digital approach offers an alternative to analog approaches such as Linvill circuits and current-conveyor-based circuits, and may offer advantages in certain applications. [4–6]. Therefore, the following considers the design of a fast-wave transmission line using digital non-Foster circuits [7].

Fast-wave transmission lines are useful in a range of applications including leaky-wave antennas, but conventional metamaterial-based designs often suffer from dispersion and bandwidth limitations [7, 8]. Non-Foster circuits can address bandwidth limitations in fast-wave lines and metamaterials [7, 9–11]. Results in [7] describe a wideband three-section fast-wave microstrip transmission line with non-Foster loading. Therefore, a digital non-Foster fast-wave design is considered below, where the three negative capacitors are replaced by digital discrete-time non-Foster circuits with negative capacitance. The following sections describe the design of digital non-Foster circuits, the fast-wave line, and simulation results for negative capacitance with limited Q (quality factor).

II. Digital Discrete-Time Non-Foster Circuit and Non-Foster Fast-Wave Microstrip Line

As noted above, the three-section fast-wave transmission line being considered requires three negative capacitors of equal value [7]. To implement these negative capacitors, consider the digital discrete-time non-Foster approach shown in Fig. 1(a). The ADC (analog-to-digital converter) with clock period T generates discrete-time signal $v_{in}[n] = v_{in}(nT)$ from the continuous-time input voltage $v_{in}(t)$. The DAC (digital-to-analog converter) with clock period T generates continuous time input current $i_{in}(t)$ from discrete-time signal $i_{in}[n] = v_{in}[n] * h[n]$, where $H(z)$ is the z-transform of $h[n]$, and $I_{in}(z) = V_{in}(z)\,H(z)$. Assuming a DAC with ZOH (zero-order hold), the input impedance is $Z_{in}(s) = V(s)/I(s) \approx V^{\star}(s)/I(s) = sT/[(1-z^{-1})H(z)]\big|_{z=e^{sT}}$ for frequencies below $0.5/T$ Hz, and where $V^{\star}(s) = \sum v(nT)e^{-nsT}$ for integer n is the starred transform [1, 12].

A simple digital negative capacitor can be implemented by approximating continuous-time relation $i_{in}(t) = C\,dv_{in}(t)/dt$ by the discrete-time relation $i_{in}[n] = C(v_{in}[n] - v_{in}[n-1])/T$ and taking the z-transform, $I_{in}(z) = C(1-z^{-1})V_{in}(z)/T$. Since $I_{in}(z) = V_{in}(z)\,H(z)$, then $H(z)$ becomes

$$H(z) = C(1-z^{-1})/T\,, \tag{1}$$

where T is the ADC and DAC clock period, and C is the desired capacitance (positive or negative) [1, 3].

A block diagram of a discrete-time negative capacitor with $C = -9.5$ pF is shown in Fig. 1(b). To accommodate Keysight ADS large-signal S-parameter simulations, analog samplers and delay lines are used to simulate the

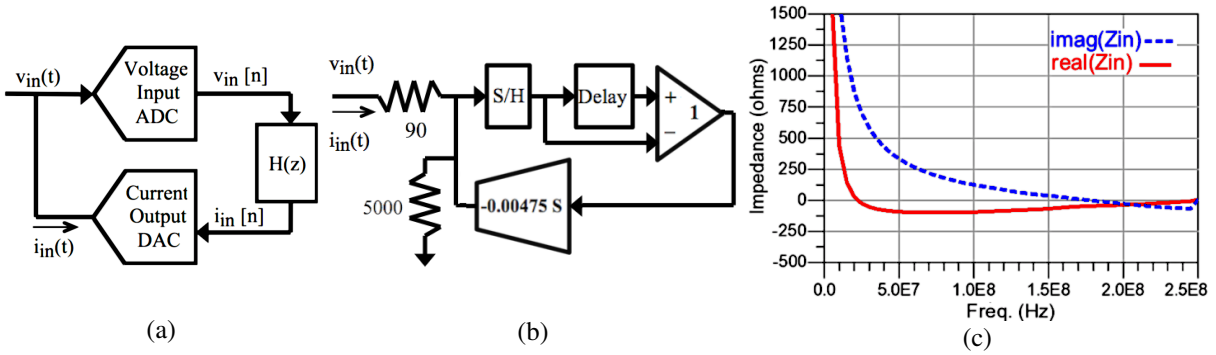

Fig. 1: (a) Block diagram of a digital discrete-time non-Foster circuit [1–3]. Input voltage $v_{in}(t)$ is converted by the ADC to $v_{in}[n]$, processed through z-transform $H(z)$, where $I_{in}(z) = V_{in}(z)\,H(z)$, to establish port current $i_{in}[n]$ to drive the DAC, where the ADC and DAC have high impedance. (b) Block diagram of a discrete-time negative capacitor with $C = -9.5$ pF. The sample-and-hold (S/H) of clock period $T = 2$ ns implements the ADC, delay line is 2 ns, and the OTA (operational transconductance amplifier) of -0.00475 S implements the DAC output current. (c) Input impedance Z_{in} for the example of Fig. 1(b), with the real part of Z_{in} shown in solid red, the imaginary part of Z_{in} in dashed blue, and $Z_{in} = -91 + j334\,\Omega$ at 50 MHz, or -9.54 pF in series with $-91\,\Omega$.

discrete-time signal processing as in [1]. The $90\,\Omega$ and $5000\,\Omega$ resistors are added to adjust Q and stability. Without the two resistors, the overall response of the circuit of Fig. 1(b) is $i_{in}[n] = -0.00475\,(v_{in}[n-1] - v_{in}[n])$. Comparison with (1) shows $C/T = -0.00475$, and thus $C = -9.5$ pF. Simulation results for the circuit of Fig. 1(b) are shown in Fig. 1(c) , confirming a negative capacitance of $C = -9.54$ pF at 50 MHz with a parasitic series resistance of $-91\,\Omega$. Stability analyses and methods to reduce parasitic resistance are given in [3] and [1].

III. Simulation Results

To demonstrate the proposed digital non-Foster approach in a fast-wave application, the three-section non-Foster fast-wave microstrip line of Fig. 2(a) was chosen. This example is based on the analog design of Long, Jacob, and Sievenpiper, and provides a baseline for comparison with the proposed digital non-Foster approach [7]. In Fig. 2(a), each of the three line sections in the dashed boxes is comprised of a pair of FR-4 microstrip lines denoted "Tx Line," with a non-Foster negative capacitance of $C = -9.5$ pF connected between the pair. In [7], each negative capacitance was previously implemented using an analog circuit. The proposed approach replaces each of the negative capacitors in Fig. 2(a) with the digital non-Foster circuit of Fig. 1(b).

The fast-wave microstrip line was simulated using the digital non-Foster implementation of Fig. 1(b) for the three negative capacitors of Fig. 2(a). Time domain transient simulations were first conducted to verify the circuit was not oscillating or latching [3]. Keysight ADS large-signal S-parameter simulation was then used to to measure the S-parameters of Fig. 2(a), with the phase of S_{21} in degrees given in Fig. 2(b), and with the magnitude of S_{21} and S_{11} in dB given in Fig. 2(c) upper plot.

In Fig. 2(b), the phase of S_{21} in degrees is plotted in solid red for Fig. 2(a). The phase of a plane wave passing through 96 mm in vacuum is plotted in dashed blue as a reference line, or "light line," as for the 100 mm line in [7]. The long-dashed green curve in Fig. 2(b) is the phase of an "ideal" version of the fast-wave microstrip of Fig. 2(a), where all three capacitors are replaced by ideal $C = -9.5$ pF capacitors in an ADS S-parameter simulation. The phase of S_{21} in Fig. 2(b) clearly exhibits the desired fast-wave characteristic, since the phase of S_{21} (solid red) remains less negative than the phase in vacuum (dashed blue), up to approximately 115 MHz. In addition, the phase of S_{21} (solid red) closely tracks the "ideal" phase (long-dashed green), up to approximately 75 MHz. (The anomalous behavior at 250 MHz in the plots corresponds to the frequency where Nyquist sampling is violated.) In the upper plot of Fig. 2(c), the magnitude of S_{21} in dB is in solid red and the magnitude of S_{11} in dB is in dashed blue. The peak of S_{21} is approximately 8.6 dB at 140 MHz, with corresponding S_{11} at 6.0 dB. Similarly, peaks of S_{21} and S_{11} greater than 0 dB were observed near 200 MHz in [7], due to gain associated with the parasitic negative resistance of the non-Foster devices.

In [7], it was also noted that the phase velocity of the fast-wave line greatly decreases when the Q of the negative capacitors falls below $Q = 2$. The $Q = |\mathrm{Im}(Z_{in})/\mathrm{Re}(Z_{in})|$ of the digital non-Foster circuit of Fig. 1(b)

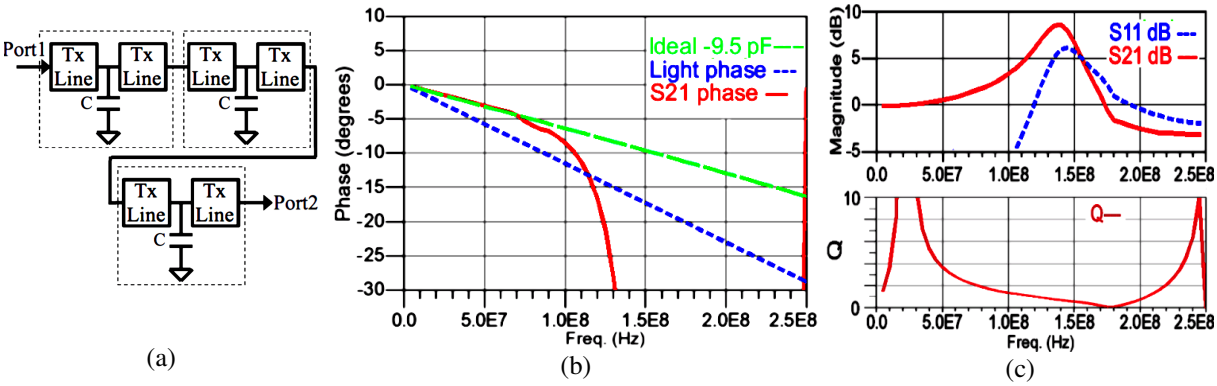

Fig. 2: (a) Block diagram of fast-wave microstrip transmission line comprised of three line sections in dashed boxes, along the lines of [7]. Each of the six "Tx Line" microstrip lines is 16 mm long and 10 mm wide on a 1.57 mm thick FR-4 substrate ($\epsilon_r = 4.4$), and the three $C = -9.5$ pF loads are Fig. 1(b) digital non-Foster circuits. (b) Phase response. Solid red line is the phase of S_{21} in degrees for Fig. 2(a), dashed blue "light line" is phase through 96 mm vacuum, long-dashed green line is an "ideal" phase reference, using ideal $C = -9.5$ pF capacitors. (c) Upper plot is magnitude in dB of S_{21} (solid red) and S_{11} (dashed blue) for Fig. 2(a). Lower plot is simulated $Q = |\text{Im}(Z_{in})/\text{Re}(Z_{in})|$ for the the $C = -9.5$ pF discrete-time negative capacitor of Fig. 1(b).

and Fig. 1(c) is plotted in Fig. 2(c) lower plot. In this, $Q > 2$ from 5 MHz to 75 MHz, and falls below unity at 115 MHz. It is observed that fast-wave behavior in the present design ceases near 115 MHz, where the phase of S_{21} (solid red line in Fig. 2(b)) first becomes more negative than the phase in vacuum (dashed blue line in Fig. 2(b)).

IV. Conclusion

A fast-wave microstrip line has been designed using digital discrete-time non-Foster circuits to implement negative capacitance. Simulation results show broadband fast-wave performance, where bandwidth appears to be limited by finite Q of the digital negative capacitors, as noted in [7]. The digital negative capacitors had $Q > 2$ from 5 MHz to 75 MHz.

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