A Two-Port Digital Discrete-Time Non-Foster Circuit Designed for Negative Capacitance

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Abstract – A digital discrete-time approach is presented for the design of two-port non-Foster circuits. The proposed digital approach offers the potential for effective implementation of complex non-Foster circuits in a wide variety of applications such as broadband metamaterials, broadband impedance matching, electrically small antennas, and artificial magnetic conductors. To illustrate the proposed digital design approach, a straightforward discrete-time implementation of a floating two-port negative capacitance is considered. Simulation results demonstrate the effectiveness of the implementation and design approach in producing -50 pF capacitance.

I. INTRODUCTION

Non-Foster circuit elements such as negative capacitors and negative inductors have recently been applied to a range of important applications such as broadband metamaterials, broadband impedance matching, electrically small antennas, and artificial magnetic conductors [1–4]. As such applications continue to show promise, there is an increasing need to develop reliable effective design approaches to explore the potential benefits of more complex non-Foster circuits. Furthermore, digital non-Foster approaches may offer performance, stability, and repeatability advantages over analog design approaches such as Linvill circuits and current-conveyor-based circuits [5–7]. Therefore, a two-port digital discrete-time implementation of a non-Foster circuit is considered [8–10]. The proposed approach provides effective implementation of complex non-Foster circuits by capitalizing on innate advantages of digital technology. In this, the voltage at each port is first digitized by an ADC (analog-to-digital converter). The desired port currents are then computed from a discrete-time admittance matrix. Finally, the port currents are established by a current-output DAC (digital-to-analog converter) at each port. Although a simple discrete-time convolution example is presented, the digital approach can also support adaptive schemes [9]. In the next section, a two-port digital discrete-time architecture is presented for the example of a floating differential negative capacitance, then the following section shows simulation results confirming the desired performance.

II. TWO-PORT DIGITAL NON-FOSTER CIRCUIT DESIGN OF A NEGATIVE CAPACITOR

As noted above, a two-port digital discrete-time implementation of a non-Foster circuit is considered [9]. For the purpose of illustration of the general approach, a two-port example is shown in Fig. 1(a). At Port 1, continuous-time signal $v_{i1}(t)$ is converted by the topmost ADC into discrete-time signal $v_{in1}[n] = v_{i1}(nT)$ for integer $n$ and sample period $T$. Similarly, the input voltage at Port 2 is converted into $v_{in2}[n] = v_{i2}(nT)$ by the lower ADC. These two discrete-time signals $v_{in1}[n]$ and $v_{in2}[n]$ undergo digital signal processing, as represented by the discrete-time admittance matrix block $Y(z)$. Finally, the continuous-time currents $i_{in1}(t)$ and $i_{in2}(t)$ at Port 1 and Port 2 are generated by the upper and lower current-output DACs, typically with ZOH (zero-order hold) and sample period $T$. Thus, the system behavior is entirely established by the discrete-time admittance matrix $Y(z)$, and the current at the two ports is then:

$$
\begin{bmatrix}
I_{in1}(z) \\
I_{in2}(z)
\end{bmatrix} = Y(z) \begin{bmatrix}
V_{in1}(z) \\
V_{in2}(z)
\end{bmatrix} = \begin{bmatrix}
Y_{11}(z) & Y_{12}(z) \\
Y_{21}(z) & Y_{22}(z)
\end{bmatrix} \begin{bmatrix}
V_{in1}(z) \\
V_{in2}(z)
\end{bmatrix}
$$

(1)

where $I_{in1}(z)$, $I_{in2}(z)$, $V_{in1}(z)$, and $V_{in2}(z)$ are the z-transforms of $i_{in1}[n]$, $i_{in2}[n]$, $v_{in1}[n]$, and $v_{in2}[n]$, respectively. The inverse z-transform yields the corresponding currents at the two ports: $i_{in1}[n] = y_{11}[n] * v_{in1}[n] + y_{12}[n] * v_{in2}[n]$ and $i_{in2}[n] = y_{21}[n] * v_{in1}[n] + y_{22}[n] * v_{in2}[n]$, where $*$ denotes convolution.
Capacitor. Furthermore, the imaginary part of the input impedance has the typical...impedance is shown in solid red, and the imaginary part of impedance the simulation is shown in Fig. 2(b), where the real part of the floating differential two-port input impedance S-parameter simulation was used to measure port impedance, and it was necessary to use samplers and delay lines the implementation outlined in Fig. 2(a) for the design equations given in (4). The Keysight ADS large-signal...S-parameter simulation was used to measure port impedance, and it was necessary to use samplers and delay lines the implementation outlined in Fig. 2(a) for the design equations given in (4). The Keysight ADS large-signal

$$I_{i1}(s) = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix} \begin{bmatrix} V_{i1}(s) \\ V_{i2}(s) \end{bmatrix} = \begin{bmatrix} sC & -sC \\ -sC & sC \end{bmatrix} \begin{bmatrix} V_{i1}(s) \\ V_{i2}(s) \end{bmatrix}$$

where $I_{i1}(s), I_{i2}(s), V_{i1}(s),$ and $V_{i2}(s)$ are the Laplace transforms of $i_{i1}(t), i_{i2}(t), v_{i1}(t),$ and $v_{i2}(t)$, respectively. The inverse Laplace transform yields the corresponding continuous-time currents at the two ports:

$$i_{i1}(t) = C \left( \frac{\partial}{\partial t} v_{i1}(t) - \frac{\partial}{\partial t} v_{i2}(t) \right) \quad \text{and} \quad i_{i2}(t) = -C \left( \frac{\partial}{\partial t} v_{i1}(t) - \frac{\partial}{\partial t} v_{i2}(t) \right)$$

where $C$ is the capacitance of the device in Fig. 1(b).

As a simple illustration, one method of implementing the two-port negative (or positive) capacitor of Fig. 1(b) is to approximate continuous-time derivatives $dv(t)/dt$, with the discrete-time form $(v_{i1}[n] - v_{i1}[n-1]) / T$. Then, the discrete-time approximation to (3) becomes $i_{i1}[n] \approx \frac{C}{T} \{(v_{i1}[n] - v_{i1}[n-1]) - (v_{i2}[n] - v_{i2}[n-1])\}$ and $i_{i2}[n] \approx \frac{-C}{T} \{(v_{i1}[n] - v_{i1}[n-1]) - (v_{i2}[n] - v_{i2}[n-1])\}$. Taking the z-transform gives the expression of the current in terms of the discrete-time admittance matrix $Y(z)$ and voltages,

$$I_{i1}(z) = Y(z) \begin{bmatrix} V_{i1}(z) \\ V_{i2}(z) \end{bmatrix} = \begin{bmatrix} C(1 - z^{-1})/T \\ -C(1 - z^{-1})/T \end{bmatrix} \begin{bmatrix} V_{i1}(z) \\ V_{i2}(z) \end{bmatrix}$$

### III. Implementation and Simulation Results

The floating two-port negative capacitance of Fig. 1(a) was simulated in the Keysight ADS simulator using the implementation outlined in Fig. 2(a) for the design equations given in (4). The Keysight ADS large-signal S-parameter simulation was used to measure port impedance, and it was necessary to use samplers and delay lines in this simulator to implement the discrete-time signal processing. The resulting differential input impedance from the simulation is shown in Fig. 2(b), where the real part of the floating differential two-port input impedance $Z_{in}$ is shown in solid red, and the imaginary part of impedance $Z_{in}$ is shown in dashed blue. At 10 MHz, the input impedance is $-91 + j314 \Omega$, and compares favorably with a predicted impedance of $+j318 \Omega$ for a $C = -50$ pF capacitor. Furthermore, the imaginary part of the input impedance has the typical $1/|\omega C|$ shape of the reactance...
A general approach has been presented for the design of a two-port digital discrete-time non-Foster circuit. Simulation results at $T = 5 \text{ ns}$ demonstrate the efficacy of the approach for a discrete-time implementation of a differential two-port $-50 \text{ pF}$ capacitance, within the capability of commercial 16-bit 200 megasample/s ADCs.

IV. CONCLUSION

A general approach has been presented for the design of a two-port digital discrete-time non-Foster circuit. Simulation results at $T = 5 \text{ ns}$ demonstrate the efficacy of the approach for a discrete-time implementation of a differential two-port $-50 \text{ pF}$ capacitance, within the capability of commercial 16-bit 200 megasample/s ADCs.

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