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A Two-Port Digital Discrete-Time Non-Foster Circuit Designed for Negative Capacitance

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***Abstract* – A digital discrete-time approach is presented for the design of two-port non-Foster circuits. The proposed digital approach offers the potential for effective implementation of complex non-Foster circuits in a wide variety of applications such as wideband metamaterials, broadband impedance matching, electrically small antennas, and artificial magnetic conductors. To illustrate the proposed digital design approach, a straightforward discrete-time implementation of a floating two-port negative capacitance is considered. Simulation results demonstrate the effectiveness of the implementation and design approach in producing -50 pF capacitance.**

I. Introduction

Non-Foster circuit elements such as negative capacitors and negative inductors have recently been applied to a range of important applications such as wideband metamaterials, broadband impedance matching, electrically small antennas, and artificial magnetic conductors [1–4]. As such applications continue to show promise, there is an increasing need to develop reliable effective design approaches to explore the potential benefits of more complex non-Foster circuits. Furthermore, digital non-Foster approaches may offer performance, stability, and repeatability advantages over analog design approaches such as Linvill circuits and current-conveyor-based circuits [5–7].

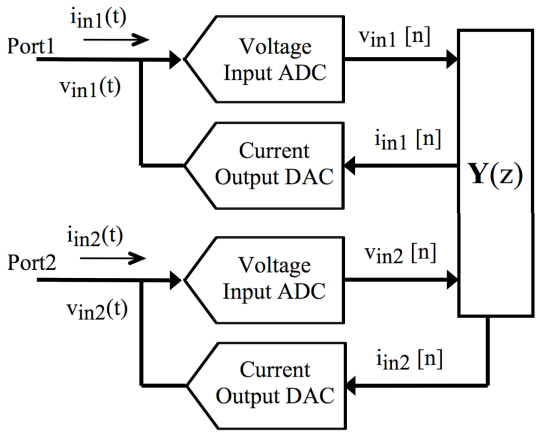
Therefore, a two-port digital discrete-time implementation of a non-Foster circuit is considered [8–10]. The proposed approach provides effective implementation of complex non-Foster circuits by capitalizing on innate advantages of digital technology. In this, the voltage at each port is first digitized by an ADC (analog-to-digital converter). The desired port currents are then computed from a discrete-time admittance matrix. Finally, the port currents are established by a current-output DAC (digital-to-analog converter) at each port. Although a simple discrete-time convolution example is presented, the digital approach can also support adaptive schemes [9]. In the next section, a two-port digital discrete-time architecture is presented for the example of a floating differential negative capacitance, then the following section shows simulation results confirming the desired performance.

II. Two-Port Digital Non-Foster Circuit Design of a Negative Capacitor

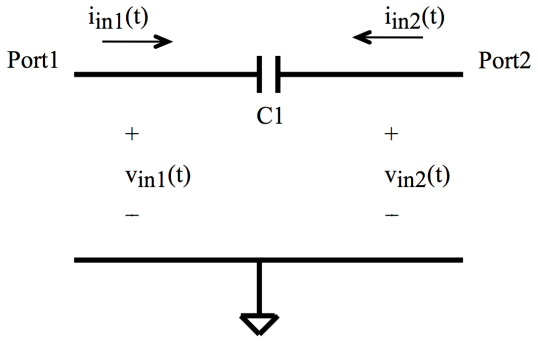
As noted above, a two-port digital discrete-time implementation of a non-Foster circuit is considered [9]. For the purpose of illustration of the general approach, a two-port example is shown in Fig. 1(a). At Port1, continuous-time signal $v_{in1}(t)$ is converted by the topmost ADC into discrete-time signal $v_{in1}[n] = v_{in1}(nT)$ for integer n and sample period T. Similarly, the input voltage at Port2 is converted into $v_{in2}[n] = v_{in2}(nT)$ by the lower ADC. These two discrete-time signals $v_{in1}[n]$ and $v_{in2}[n]$ undergo digital signal processing, as represented by the discrete-time admittance matrix block $\boldsymbol{Y}(z)$. Finally, the continuous-time currents $i_{in1}(t)$ and $i_{in2}(t)$ at Port1 and Port2 are generated by the upper and lower current-output DACs, typically with ZOH (zero-order hold) and sample period T. Thus, the system behavior is entirely established by the discrete-time admittance matrix $\boldsymbol{Y}(z)$, and the current at the two ports is then:

$$\begin{bmatrix} I_{in1}(z) \\ I_{in2}(z) \end{bmatrix} = \mathbf{Y}(z) \begin{bmatrix} V_{in1}(z) \\ V_{in2}(z) \end{bmatrix} = \begin{bmatrix} Y_{11}(z) & Y_{12}(z) \\ Y_{21}(z) & Y_{22}(z) \end{bmatrix} \begin{bmatrix} V_{in1}(z) \\ V_{in2}(z) \end{bmatrix} \tag{1}$$

where $I_{in1}(z)$, $I_{in2}(z)$, $V_{in1}(z)$, and $V_{in2}(z)$ are the z-transforms of $i_{in1}[n]$, $i_{in2}[n]$, $v_{in1}[n]$, and $v_{in2}[n]$, respectively. The inverse z-transform yields the corresponding currents at the two ports: $i_{in1}[n] = y_{11}[n] * v_{in1}[n] + y_{12}[n] * v_{in2}[n]$ and $i_{in2}[n] = y_{21}[n] * v_{in1}[n] + y_{22}[n] * v_{in2}[n]$, where $*$ denotes convolution.



(a)



(b)

Fig. 1: (a) Block diagram of a two-port digital discrete-time non-Foster circuit [8, 9]. The input voltages at each port are converted by each ADC, processed through discrete-time admittance matrix $\mathbf{Y}$ to establish port currents with each DAC, where the ADC and DAC devices have high impedance. (b) Example non-Foster two-port circuit consisting of a single floating negative capacitor C1, with capacitance C, and connected between the two ports.

To illustrate the design of a digital discrete-time implementation of a non-Foster circuit using the scheme of Fig. 1(a), a two-port floating negative capacitor design is considered. In the circuit of Fig. 1(b), a two-port network consisting of a single negative capacitor will be implemented, where the negative capacitor is connected between Port1 and Port2. The circuit of Fig. 1(b) is chosen to demonstrate the effectiveness of the design approach, because the expected performance goals are straightforward and clearly defined. For the analog circuit of Fig. 1(b), currents are related to voltages through the continuous-time admittance matrix [11]:

$$\begin{bmatrix} I_{in1}(s) \\ I_{in2}(s) \end{bmatrix} = \begin{bmatrix} Y_{11}(s) & Y_{12}(s) \\ Y_{21}(s) & Y_{22}(s) \end{bmatrix} \begin{bmatrix} V_{in1}(s) \\ V_{in2}(s) \end{bmatrix} = \begin{bmatrix} sC & -sC \\ -sC & sC \end{bmatrix} \begin{bmatrix} V_{in1}(s) \\ V_{in2}(s) \end{bmatrix} \tag{2}$$

where $I_{in1}(s)$, $I_{in2}(s)$, $V_{in1}(s)$, and $V_{in2}(s)$ are the Laplace transforms of $i_{in1}(t)$, $i_{in2}(t)$, $v_{in1}(t)$, and $v_{in2}(t)$, respectively. The inverse Laplace transform yields the corresponding continuous-time currents at the two ports:

$$i_{in1}(t) = C\left(\frac{\partial}{\partial t}v_{in1}(t) - \frac{\partial}{\partial t}v_{in2}(t)\right) \text{ and } i_{in2}(t) = -C\left(\frac{\partial}{\partial t}v_{in1}(t) - \frac{\partial}{\partial t}v_{in2}(t)\right), \tag{3}$$

where C is the capacitance of the device in Fig. 1(b).

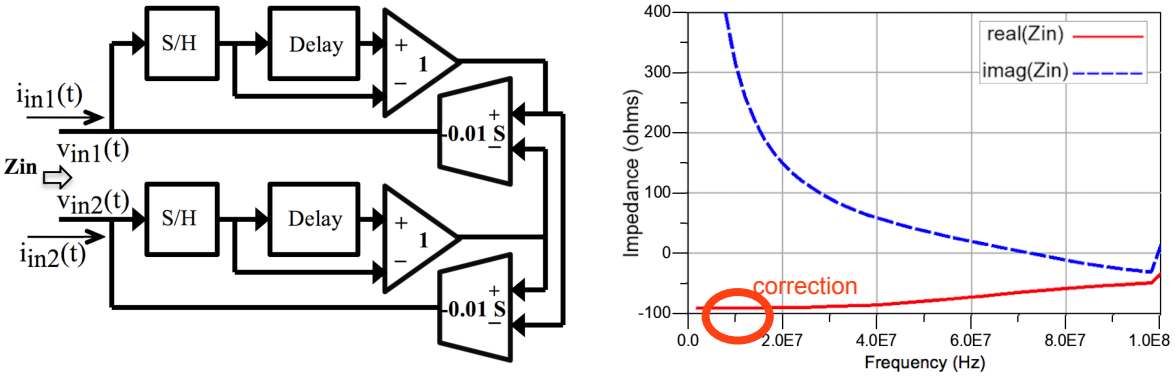
As a simple illustration, one method of implementing the two-port negative (or positive) capacitor of Fig. 1(b) is to approximate continuous-time derivatives $dv(t)/dt$, with the discrete-time form $(v_{in}[n] - v_{in}[n-1])/T$. Then, the discrete-time approximation to (3) becomes $i_{in1}[n] \approx \frac{C}{T}\{(v_{in1}[n] - v_{in1}[n-1]) - (v_{in2}[n] - v_{in2}[n-1])\}$ and $i_{in2}[n] \approx \frac{-C}{T}\{(v_{in1}[n] - v_{in1}[n-1]) - (v_{in2}[n] - v_{in2}[n-1])\}$. Taking the z-transform gives the expression of the current in terms of the discrete-time admittance matrix $\mathbf{Y}(z)$ and voltages,

$$\begin{bmatrix} I_{in1}(z) \\ I_{in2}(z) \end{bmatrix} = \mathbf{Y}(z) \begin{bmatrix} V_{in1}(z) \\ V_{in2}(z) \end{bmatrix} = \begin{bmatrix} C(1-z^{-1})/T & -C(1-z^{-1})/T \\ -C(1-z^{-1})/T & C(1-z^{-1})/T \end{bmatrix} \begin{bmatrix} V_{in1}(z) \\ V_{in2}(z) \end{bmatrix}. \tag{4}$$

III. Implementation and Simulation Results

The floating two-port negative capacitance of Fig. 1(a) was simulated in the Keysight ADS simulator using the implementation outlined in Fig. 2(a) for the design equations given in (4). The Keysight ADS large-signal S-parameter simulation was used to measure port impedance, and it was necessary to use samplers and delay lines in this simulator to implement the discrete-time signal processing. The resulting differential input impedance from the simulation is shown in Fig. 2(b), where the real part of the floating differential two-port input impedance Z_{in} is shown in solid red, and the imaginary part of impedance Z_{in} is shown in dashed blue. At 10 MHz, the input impedance is $-91 - j314\,\Omega$, and compares favorably with a predicted impedance of $+j318\,\Omega$ for a $C = -50$ pF capacitor. Furthermore, the imaginary part of the input impedance has the typical $1/|\omega C|$ shape of the reactance

correction



(a) (b)

Fig. 2: (a) Block diagram of a discrete-time two-port negative capacitor with $C = -50$ pF, using analog samplers and delay lines to implement the discrete-time signal processing. The two sample-and-hold blocks (S/H) with clock period $T = 5$ ns generate sampled input voltages $v_{in1}[n]$ and $v_{in2}[n]$. Analog time delays of $T = 5$ ns produce $v_{in1}[n-1]$ and $v_{in2}[n-1]$. Operational transconductance amplifiers (OTA) have transconductance of -0.01 S [12]. The top OTA generates Port1 current $i_{in1}[n] = -0.01\,\{(v_{in1}[n] - v_{in1}[n-1]) - (v_{in2}[n] - v_{in2}[n-1])\}$, and the bottom OTA generates $i_{in2}[n] = -i_{in1}[n]$. Comparison with (4) shows $C/T = -0.01$, so $C = -50$ pF. (b) Differential two-port input impedance Z_{in} for Fig. 2(a), using Keystone ADS large-signal S-parameter simulation. The real part of the Z_{in} of Fig. 2(a) is shown in solid red, and the imaginary part is shown in dashed blue. The observed impedance of $-91 + j314\,\Omega$ at 10 MHz is near the predicted impedance of $+j318\,\Omega$ for $C = -50$ pF.

of a capacitor, except with inverted sign due to the negative capacitance. The anomalous impedance and abrupt change at 100 MHz is at the Nyquist frequency $0.5/T$, where the sampling theorem is not satisfied. Stability analyses and methods to reduce parasitic resistance are given for a similar one-port in [10] and [8].

IV. Conclusion

A general approach has been presented for the design of a two-port digital discrete-time non-Foster circuit. Simulation results at $T = 5$ ns demonstrate the efficacy of the approach for a discrete-time implementation of a differential two-port -50 pF capacitance, within the capability of commercial 16-bit 200 megasample/s ADCs.

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References

[1] S. Hrabar, I. Krois, I. Bonic, and A. Kiricenko, "Negative capacitor paves the way to ultra-broadband metamaterials," *Applied Physics Letters*, vol. 99, no. 25, p. 254103, 2011.
[2] D. Gregoire, C. White, and J. Colburn, "Wideband artificial magnetic conductors loaded with non–Foster negative inductors," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1586–1589, 2011.
[3] S. Sussman-Fort and R. Rudish, "Non-Foster impedance matching of electrically-small antennas," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 8, pp. 2230–2241, Aug. 2009.
[4] N. Zhu and R. Ziolkowski, "Active metamaterial-inspired broad-bandwidth, efficient, electrically small antennas," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1582–1585, 2011.
[5] A. Sedra and K. Smith, "A second-generation current conveyor and its applications," *IEEE Trans. Circuit Theory*, vol. 17, no. 1, pp. 132–134, 1970.
[6] J. Linvill, "Transistor negative-impedance converters," *Proc. of the IRE*, vol. 41, no. 6, pp. 725–729, Jun. 1953.
[7] S. Stearns, "Incorrect stability criteria for non-Foster circuits," in *IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Jul. 2012, pp. 1–2.
[8] T. Weldon, J. Covington, K. Smith, and R. Adams, "Performance of digital discrete-time implementations of non-Foster circuit elements," in *2015 IEEE Int. Symp. on Circuits and Systems (ISCAS)*, in press, May 2015, pp. 1–4.
[9] T. P. Weldon, "Digital discrete-time non-Foster circuits and elements," International Patent Application No. PCT/US2015/27789, Apr. 27, 2015.
[10] T. Weldon, J. Covington, K. Smith, and R. Adams, "Stability conditions for a digital discrete-time non-Foster circuit element," in *IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Jul. 2015, in press.
[11] R. Ludwig and G. Bogdanov, *RF Circuit Design: Theory & Applications, 2/E*, 2nd ed., Prentice Hall, 2009.
[12] R. J. Baker , H. W. Li and D. E. Boyce, *CMOS Circuit Design, Layout and Simulation,*, IEEE Press, 1998.