A Clock-Tuned Discrete-Time Negative Capacitor Implemented Using Analog Samplers

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***Abstract*—The recent introduction of digital non-Foster circuits offers new methods for implementing negative capacitance and inductance, but may require a high-speed high-resolution digital signal processor, analog-to-digital converter, and digital-to-analog converter. Therefore, an alternative discrete-time design approach is presented, where a clock-tuned negative capacitor is implemented using analog samplers. The resulting design requires only two samplers, a differential amplifier, and an operational transconductance amplifier, eliminating the need for a digital signal processor and converters. In addition, it is shown that the negative capacitance can be tuned by the digital clock and is theoretically proportional to the clock period. Experimental results for a prototype demonstrate a tunable capacitance from -2.1 nF to -5.5 nF with $|Q| > 2$ for signal frequencies below approximately one-tenth of the clock frequency.**

I. Introduction

There is renewed interest in the design of non-Foster circuits such as negative capacitors to support important and emerging applications such as electrically-small antennas, metamaterial cloaks, and software defined radios [1]–[5]. Although some successful results have been obtained with analog non-Foster circuits, design issues such as stability remain quite challenging [6], [7]. Recently, digital non-Foster circuits have shown promise as an alternative design approach that may leverage advantages of digital technology for certain applications [8]–[10]. One key advantage of the digital approach is that the Nyquist limit sets an upper frequency bound for any potential instability. However, digital non-Foster circuits may be limited by the need for a high-speed high-resolution digital signal processor, high-speed ADC (analog-to-digital converter), and high-speed DAC (digital-to-analog converter).

Therefore, an alternative discrete-time implementation of a digital non-Foster circuit is proposed, where a clock-tuned negative capacitor is implemented using analog samplers, without a signal processor, ADC, or DAC. The proposed circuit consists of two analog samplers, a differential amplifier, and an OTA (operational transconductance amplifier). The clock and a delayed clock set the timing for the samplers, and the frequency of the clock sets the desired capacitance. Although a similar clock-tuned digital non-Foster circuit was given in [11], it required an ADC and DAC. Lastly, depending on the application and implementation, the simplicity and analog nature of the proposed approach may offer the designer advantages in chip area, power consumption, bandwidth, or signal dynamic range.

In Section II, theory is presented for the clock-tuned digital negative capacitor. Section III describes simulations and measured results for a prototype, demonstrating a negative capacitance can be clock-tuned from -2.6 nF to -6.2 nF.

II. Theory

The proposed implementation of the clock-tuned discrete-time negative capacitor is shown in Fig. 1, where $v_{in}(t)$ is the input voltage, $i_{in}(t)$ is the input current of the system, and *Clk1* and *Clk2* are digital clock signals at the discrete-time sampling frequency $f_s = 1/T_s$. The input signal is sampled by a first analog sampler producing discrete-time signal $v_{in}[n] = v_{in}(nT_s)$. This first sampled signal is then sampled by the second analog sampler to produce $v_{in}[n-1]$. The output of the difference amplifier is then $v_{in}[n] - v_{in}[n-1]$, and the output of the OTA becomes the input current of the system $i_{in}(nT_s) = i_{in}[n] = g_m \cdot (v_{in}[n] - v_{in}[n-1])$, where g_m is the OTA tranconductance.

The timing diagram for the two clock signals of Fig. 1 is shown in Fig. 2. The signal *Clk1* provides the clock for the first sampler, while *Clk2* provides the clock signal for the second sampler, with both signals at frequency f_s. In the prototype,

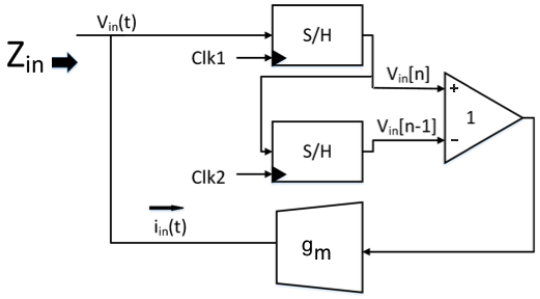

Fig. 1. Block diagram of proposed system, where "Clk1" and "Clk2" are the sampling clocks.

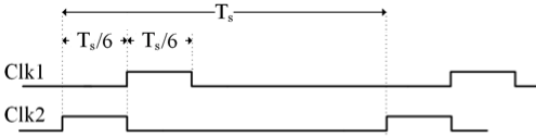

Fig. 2. Timing diagram of proposed system, where "Clk1" and "Clk2" are the sampling clocks at frequency $f_s = 1/T_s$, and where the pulse width was chosen to be $T_s/6$ to accommodate board and device limitations.

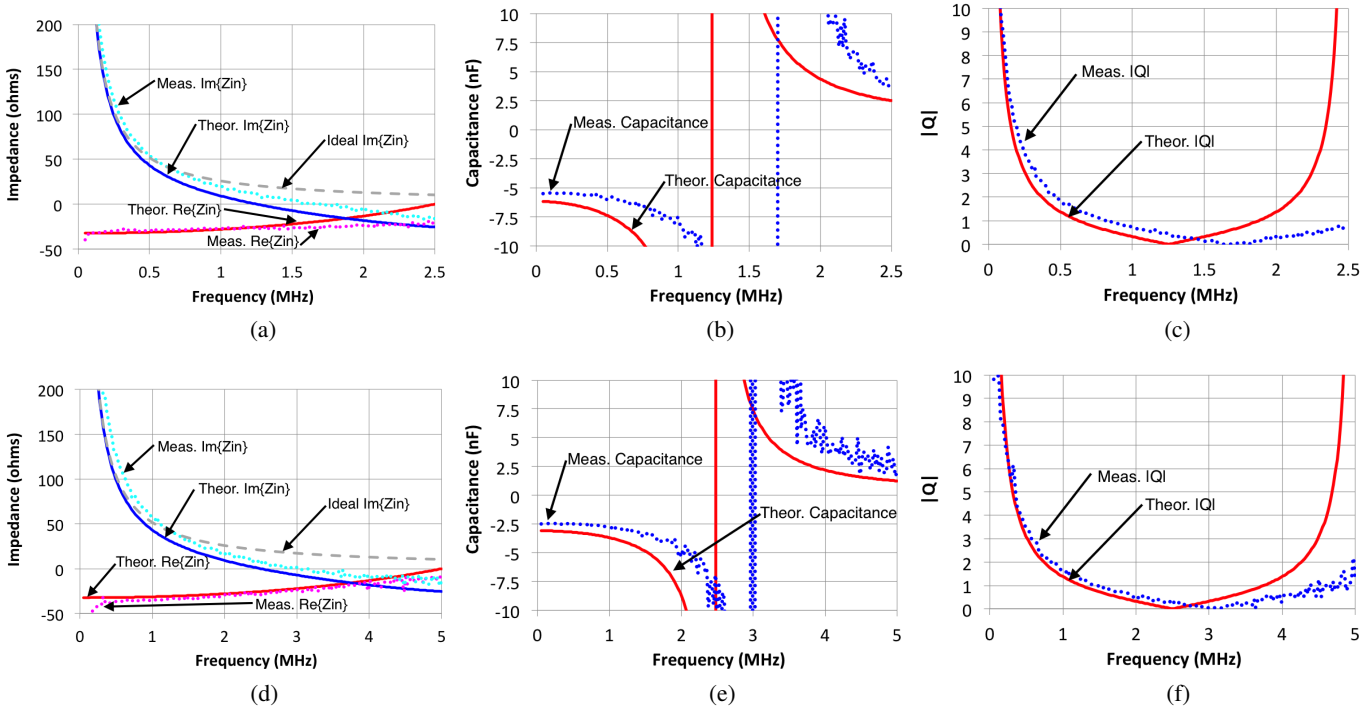

Fig. 3. Theoretical and measured prototype data for clocks of $f_s = 5$ MHz (upper) and $f_s = 10$ MHz (lower). Upper three plots show measured results for clock frequency $f_s = 5$ MHz: (a) measured (dotted curves) and theoretical (solid curves) $Re\{Z_{in}\}$ and $Im\{Z_{in}\}$, (b) measured (dotted curves) and theoretical (solid curves) capacitance, and (c) measured (dotted curve) and theoretical (solid curve) quality factor $|Q| = |Im\{Z_{in}\}/Re\{Z_{in}\}|$. Lower three plots are measured results for clock frequency $f_s = 10$ MHz: (d) measured (dotted curves) and theoretical (solid curves) $Re\{Z_{in}\}$ and $Im\{Z_{in}\}$, (e) measured (dotted curves) and theoretical (solid curves) capacitance, and (f) measured (dotted curve) and theoretical (solid curve) quality factor $|Q| = |Im\{Z_{in}\}/Re\{Z_{in}\}|$.

track-and-hold samplers were employed, such that the output of the first stage tracks the input while *Clk1* is high. *Clk2* causes the second stage to sample the output from the first sample and hold stage, just before a new input sample is acquired by the first stage. Note that while *Clk2* is high, the two sampler outputs are equal, and the OTA output current becomes zero. This momentary zero of the output results in a effective duty cycle, denoted $D = 5/6$ for the timing in Fig. 2. Although the timing of Fig. 2 with $D = 5/6$ was chosen to meet constraints of available hardware, it also serves to demonstrate the efficacy of the proposed system even with imperfect samplers. Faster samplers, timing, or circuit design implementations may approach the ideal case with $D = 1$.

A capacitive input impedance at $v_{in}(t)$ can be generated using the discrete-time approximation of the derivative. The current of a capacitor $i(t) = C\, dv(t)/dt$ is approximated using sampler outputs $v_{in}[n]$ and $v_{in}[n-1]$ in Fig. 1 such that

$$i_{in}[n] \approx C\, \frac{v_{in}[n] - v_{in}[n-1]}{T_s}\,, \tag{1}$$

where $v_{in}[n]$ is the sampled input voltage, $i_{in}[n] = i_{in}(nT_s)$ is the OTA current in amperes, C is the design capacitance in Farads, T_s is the sampling period in seconds, and where other effects such as undesired attenuation of the sampled signal could also be included above.

In Fig. 1, the current generated by the OTA including the effect of duty cycle is then

$$i_{in}[n] = g_m\, D\, \{v_{in}[n] - v_{in}[n-1]\}\,, \tag{2}$$

where duty cycle D is the portion of the clock period where the output current is nonzero, and g_m is the transconductance of the OTA in Siemens. Then, comparing (1) and (2) and solving for C yields

$$C \approx D \cdot g_m \cdot T_s = D \cdot g_m / f_s\,, \tag{3}$$

where C may be a positive or negative capacitance, and C is inversely proportional to clock frequency $f_s = 1/T_s$. Also note that from [8], the input impedance $Z_{in}(s)$ seen at the input port of Fig. 1 can be expressed as

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \frac{sT_s}{(1 - z^{-1})\, H\,(z)}\,\bigg|_{z=e^{sT_s}}\,, \tag{4}$$

where $H(z) = I_{in}(z)/V_{in}(z)$ is found by taking the z-transform of (1), yielding

$$H\,(z) = \frac{I_{in}(z)}{V_{in}(z)} \approx \left(1 - z^{-1}\right) \cdot \frac{C}{T_S}\,, \tag{5}$$

where C is the desired capacitance seen at the input port of Fig. 1.

III. Prototype Measurements

In this section, theoretical results from (4) are compared with measured results from the hardware prototype. Fig. 3 shows theoretical and measured results for a prototype of Fig. 1, with design parameters $g_m \approx -0.037$ S and $D = 5/6$. For the upper plots of Fig. 3(a)–(c), the digital sampling clock frequency is $f_s = 5$ MHz, resulting in a theoretical capacitance of $C = -6.17$ nF. For the lower plots of Fig. 3(d)–(f), the

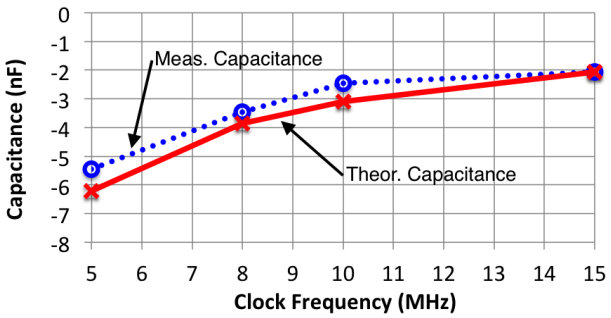

Fig. 4. Theoretical and measured capacitance as a function of clock frequency. Solid red curve is theoretical capacitance, dotted blue is measured low-frequency capacitance, showing capacitance inversely proportional to clock frequency.

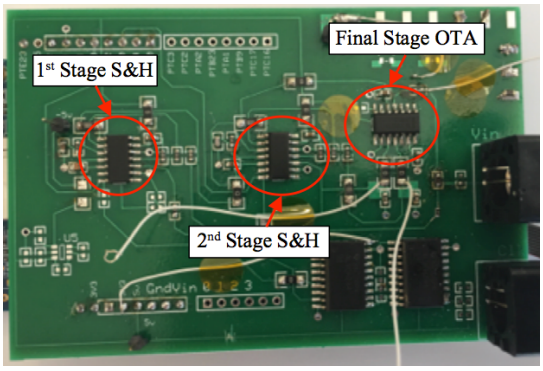

Fig. 5. Prototype showing location of various components.

digital sampling clock frequency is $f_s = 10$ MHz, resulting in a theoretical capacitance of $C = -3.08$ nF. Measured results required a 20 nF capacitor in parallel with the input, plus a bias tee with less than 100 ohm dc circuit loading for stabilization of the network analyzer measurement. The effects of the 20 nF stabilization capacitor and board stray capacitance were removed in computing the measured impedance Z_{in}.

The measured real and imaginary impedance Z_{in} of the prototype with $f_s = 5$ MHz are given in Fig. 3(a) for the prototype of Fig. 5, along with theoretical Z_{in} from (4). The dotted magenta curve shows the measured real component $Re(Z_{in})$ and the dotted cyan curve shows the imaginary component $Im(Z_{in})$ of the measured input impedance. The solid red and solid blue curves show the real and imaginary components of the theoretical Z_{in} from (4). The gray dashed curve is the reactance of a $C = -6.2$ nF ideal capacitor. The measured impedance closely follows the the theoretical impedance at low frequency, up to approximately one-tenth of the clock frequency, or 0.5 MHz. At higher frequencies, some degradation is expected, especially for low impedances where the OTA of Fig. 1 may be current limited.

The measured effective capacitance with $f_s = 5$ MHz is shown in Fig. 3(b) as a function of input frequency along with the theoretical capacitance. The dotted blue curve is the measured value of effective capacitance $C_{eff} = -1/[2\pi f Im(Z_{in})]$, and the solid red curve is the theoretical effective capacitance computed from (4). At low frequency, the measured effective capacitance is -5.5 nF, and the theoretical capacitance is $C = -6.2$ nF for the $f_s = 5$ MHz clock. In addition, Fig. 3(c) shows the magnitude of the quality factor $|Q| = |Im(Z_{in})/Re(Z_{in})|$ as a function of input frequency, with the solid red curve being theoretical $|Q|$, and dotted blue measured $|Q|$. The measured $|Q|$ closely follows the the theoretical, with measured $|Q|$ greater than 2, up to approximately one-tenth of the clock frequency, or 0.5 MHz (more precisely, $|Q|$=2.0 at 0.48 MHz).

To observe the clock-tuning of capacitance, measurements at sample clock frequency $f_s = 10$ MHz are given in Fig. 3(d)-(f). The measured impedance Z_{in} of the prototype with $f_s = 10$ MHz is given in Fig. 3(d), along with theoretical Z_{in}. The dotted magenta curve shows the real component $Re(Z_{in})$ and the dotted cyan curve shows the imaginary component $Im(Z_{in})$ of the measured input impedance. The solid red and solid blue curves show the real and imaginary components of the theoretical Z_{in} from (4). The gray dashed curve is the reactance of a $C = -3.1$ nF ideal capacitor. The measured impedance closely follows the the theoretical impedance at low frequency, up to approximately one-tenth of the clock frequency, or 1 MHz. Again, some degradation is expected at higher frequencies, where the OTA of Fig. 1 may be current limited.

The measured effective capacitance with $f_s = 10$ MHz is shown in Fig. 3(e) as a function of input frequency along with the theoretical capacitance. The dotted blue curve is the measured value of effective capacitance $C_{eff} = -1/[2\pi f Im(Z_{in})]$, and the solid red curve is the theoretical effective capacitance computed from (4). At low frequency, the measured effective capacitance is -2.5 nF, and the theoretical capacitance is $C = -3.1$ nF for the $f_s = 10$ MHz clock. Fig. 3(f) shows the magnitude of the quality factor $|Q|$ as a function of input frequency, with the solid red curve being theoretical $|Q|$, and dotted blue measured $|Q|$. The measured $|Q|$ closely follows the the theoretical, with measured $|Q|$ greater than 2, up to almost one-tenth of the clock frequency, or 1 MHz (more precisely, $|Q|$=2.0 at 0.84 MHz). Importantly, the value of the low-frequency capacitance is approximately reduced by half as the clock frequency was doubled from $f_s = 5$ MHz to $f_s = 10$ MHz, in agreement with (3).

Fig. 4 shows theoretical and measured capacitance as a function of clock frequency., with data points at 5, 8, 10, and 15 MHz. The solid red curve is theoretical capacitance $C_{eff} = -1/[2\pi f Im(Z_{in})]$ from (4), and the dotted blue is measured low-frequency ($\approx$100 kHz) capacitance $C_{eff} = -1/[2\pi f Im(Z_{in})]$. The results show measured capacitance approximately inversely proportional to clock frequency, ranging from -2.1 nF at $f_s = 15$ MHz to -5.5 nF at $f_s = 5$ MHz. The theoretical capacitance ranged from -2.1 nF at $f_s = 15$ MHz to -6.2 nF at $f_s = 5$ MHz. The modest difference between theory and measurements is thought to be caused by a fairly large nonlinear variation of g_m inherent in the OPA615 OTA, combined with unavoidable internal signal amplitude variations with changing signal and clock frequencies when approximating the derivative of the input voltage.

The prototype is shown in Fig. 5. The components are laid

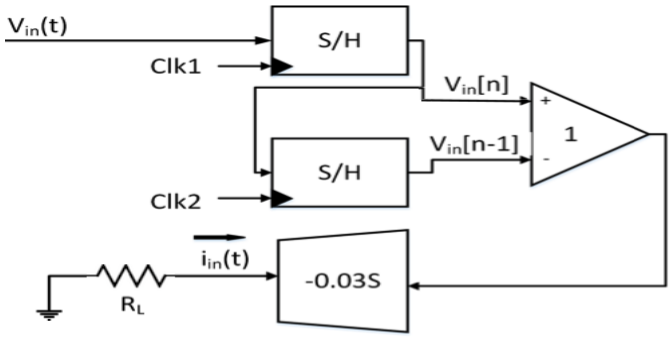

Fig. 6. Block diagram of open-loop configuration of proposed system for initial testing. Output stage is driving a resistive load, R_L. Note that to maintain consistency in current notation, the simulated and measured current in this configuration is relative to the direction indicated by $i_{in}(t)$.

out on an Arduino-style shield board that interfaces with a FRDM-K64F to generate the clock timing of Fig. 2 for *Clk1* and *Clk2*. The board consists of three primary components, all of which are configurations of the OPA615 integrated circuit. The two clocked sample and hold blocks of Fig. 1 are implemented using two OPA615 devices. A third OPA615 device implements the differential amplifier and OTA block of Fig. 1.

The time-domain open-loop characteristics of the prototype of the system of Fig. 1 were also measured, and compared to simulated results on the Keysight ADS simulator. For the open-loop testing, a resistive load R_L was placed at the OTA output, resulting in the open-loop configuration of Fig 6.

Open-loop simulation results are shown in Fig. 7 for sampling clock frequency $f_s = 10$ MHz, duty cycle $D = 5/6$, and $R_L = 500$ ohms. The blue curve is $v_{in}(t)$, red signal is $v_{in}[n]$, solid green is $v_{in}[n-1]$, and magenta is $i_{in}(t)$. Observe that during one-sixth of each clock cycle the current is zero, because $v[n] = v[n-1]$ during this time interval (to accommodate timing limitations of the prototype and samplers).

Open-loop measured results are shown in Fig. 8 for sampling clock frequency $f_s = 10$ MHz, duty cycle $D = 5/6$, and $R_L = 500$ ohms. As before, the blue curve is $v_{in}(t)$, red signal is $v_{in}[n]$, solid green is $v_{in}[n-1]$, and magenta is $i_{in}(t)$. Most importantly, the measured results of Fig. 8 closely resemble the simulation results of Fig. 7.

IV. Conclusion

A clock-tuned discrete-time negative capacitor design approach has been presented using analog samplers. Prototype measurements confirm a tuning range from -2.1 nF with a 15 MHz clock, to -5.5 nF with a $f_s = 5$ MHz clock. The results compare favorably with a theoretical capacitance range of -2.1 nF to -6.2 nF for the same clocking. It is suspected that the slight difference between theory and measurement may be caused by nonlinear dependence of transconductance with signal amplitude inherent with the OTA, combined with the large signal variations over frequency expected for a capacitance or differentiator circuit. Nevertheless, useful variable negative capacitance was observed, with useful

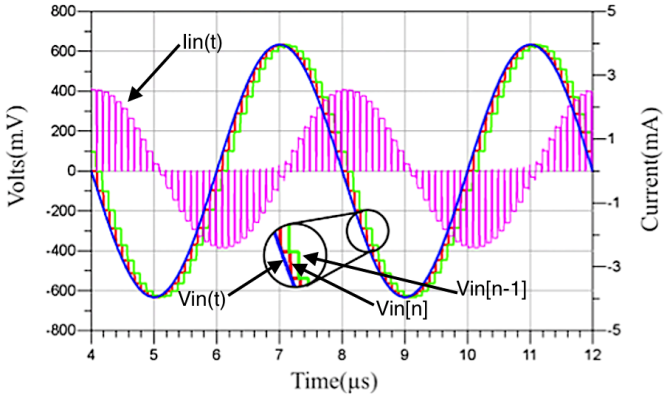

Fig. 7. Simulation results showing open-loop time-domain waveforms of Fig. 6. The simulation results include the input signal, $v_{in}(t)$, the output of the first sample stage,$v_{in}[n]$, the output of the second sample stage,$v_{in}[n-1]$, and the output current of the OTA, $i_{in}(t)$, with clock $f_s = 10$ MHz, duty cycle $D = 5/6$, and $R_L = 500$ ohms.

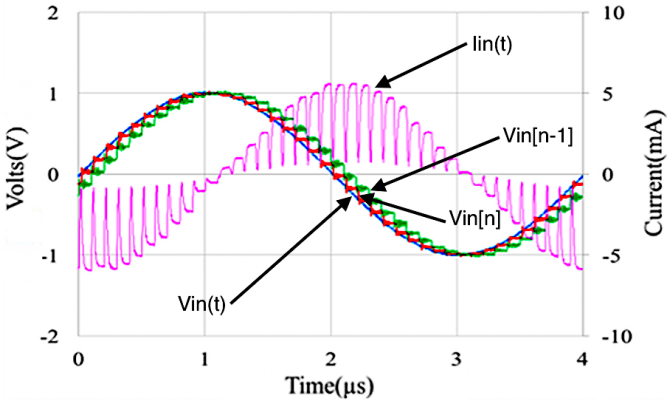

Fig. 8. Measured results showing open-loop time-domain waveforms of Fig. 6. The measurement results include the input signal, $v_{in}(t)$, the output of the first sample stage,$v_{in}[n]$, the output of the second sample stage,$v_{in}[n-1]$, and the output current of the OTA, $i_{in}(t)$, with clock $f_s = 10$ MHz, duty cycle $D = 5/6$, and $R_L = 500$ ohms.

signal-frequency range up to approximately one-tenth of the clock frequency. Beyond one-tenth of the clock frequency, the $|Q|$ of the capacitor falls below 2. Current board layout and limitations of laboratory equipment hindered measurements at higher and lower clock frequencies. Lastly, note that the negligible current of the samplers was not included in the theory, because the sampler input impedances are 200 kΩ in parallel with 1.2 pF, and thus much smaller than the ≈nF range of the prototype.

Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. 1731675.

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