A Clock-Tuned Digital Memristor Emulator

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***Abstract*—Memristors are inherently frequency-dependent devices that may be limited by a variety of practical constraints such as operating frequency ranges of commercially available devices, or complexity of analog circuit implementations that emulate memristor behavior. Therefore, a novel clock-tuned digital memristor emulator is presented, where the frequency-dependent behavior of the memristor can be tuned over a range of two decades. An external clock provides simple adjustment of the operating frequency range and frequency-dependent behavior of the memristor, without requiring any modification of firmware or hardware. The digital memristor is implemented in embedded software on a microcontroller with an integrated analog-to-digital and digital-to-analog converter, providing a reconfigurable platform that can support other non-ideal memristor characteristics. Measurements of a prototype demonstrate a clock-tuned memristor with pinched hysteresis loop v–i curves that are unchanged over an operating frequency range of 100:1.**

I. Introduction

Memristors have been the subject of intense investigation during the past few years, due to their potential to transform diverse applications such as computer memory, data storage, antennas, and neuromorphic computing [1]–[7]. Typically, memristors have a frequency-dependent response with resistance determined by a flux or charge, and are characterized by the presence of a *pinched hysteresis loop* in the v–i plot and [8]–[11]. Although many investigators have recently focused on inventing elementary devices such as in [2], others have developed circuits that emulate memristor behavior [12]–[17]. Because of limited availability and capability of commercial memristors, circuits that emulate memristors continue to play an important role in developing new memristor applications and in exploring novel types of theoretical memristors.

Since the behavior of memristors is frequency dependent [18], it is advantageous to be able to tune a memristor such that desired characteristics (such as a particular desired v–i curve) may occur at some specific frequency for an application. Therefore, a novel clock-tuned digital memristor is presented, where the frequency-dependent behavior of the memristor can be tuned over a range of two decades using an external clock. The proposed memristor is digitally implemented using embedded software on an MCU (microcontroller unit) with an integrated ADC (analog-to-digial converter) and DAC (digital-to-analog converter). Compared to prior digital memristor emulators in [14]–[16], the proposed approach provides simple clock tuning without requiring any modification of firmware or hardware, and does not require a switched-resistor network nor the use of a digital potentiometer. In addition, clock-tuning may enable adaptively-tuned applications. Lastly, the embedded software should be modifiable to emulate other non-ideal memristors noted in [9].

Section II presents theory for the clock-tuned digital memristor. Section III describes simulations and measured results for a prototype, demonstrating a tuning range of two decades.

II. Theory

A memristor is a two-terminal device with voltage and current described by a state-dependent Ohm's law [9]. The memristance is typically defined by some combination of voltage v, current i, electric charge $q = \int i(t)\,dt$, and flux $\varphi = \int v(t)\,dt$ [3]. In this paper, we consider an ideal voltage-controlled memristor (also referred to as flux-controlled memristor) defined by [11]

$$i(t) = v(t)\,G(\varphi) = K_G \frac{v(t)}{\varphi(t)} \tag{1}$$

$$\varphi(t) = \varphi(0) + \int_0^t v(\tau)\,d\tau\,, \tag{2}$$

where the memconductance is $G(\varphi) = K_G/\varphi(t)$, $\varphi(t)$ is the flux, $v(t)$ is the voltage across the memristor, $i(t)$ is the current through the memristor, and K_G is a constant scale factor.

The block diagram of the proposed clock-tuned memristor is shown in Fig. 1, where the input digital clock signal "clk" at frequency $f_c = 1/T_c$ is used for tuning. The input voltage $v(t)$ is converted to discrete-time signal $v[n] = v(nT_c)$ by the ADC, before being digitally processed by the MCU to form $v_{dac}[n]$ and DAC output voltage $v_{dac}(t)$. The memristor current is then $i(nT_c) = i[n] = (v[n] - v_{dac}[n])/R_{dac}$.

The flux $\varphi(t)$ from (2) can be approximated for the digital memristor as $\varphi(nT_c) = \varphi[n] \approx \varphi[n-1] + T_c v[n]$, where $\varphi[0] = \varphi_\circ$ is the initial flux. Then, $G[n] =$

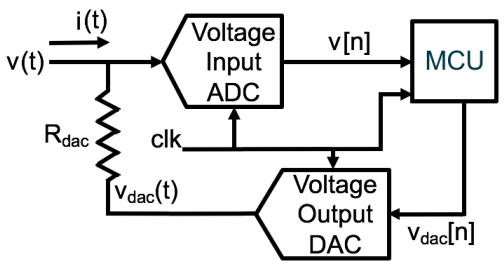

Fig. 1. Block diagram of proposed clock-tuned digital memristor, where $v(t)$ is the memristor voltage, $i(t)$ is memristor current, "clk" is the digital clock input, and where the clock-controlled architecture is similar to [19].

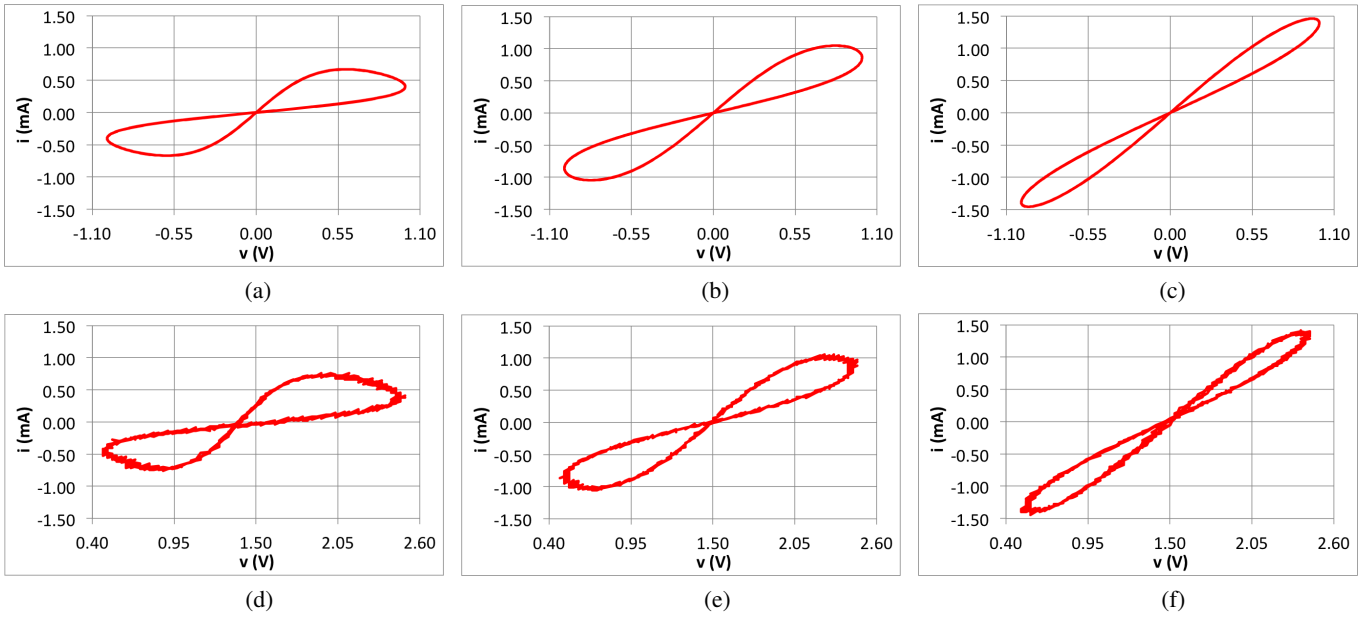

Fig. 2. Simulated and measured pinched hysteresis loops with 5 kHz clock. Upper three pinched hysteresis loop v–i plots are simulations for 1 V peak input sine wave at: (a) 10 Hz, (b) 30 Hz, and (c) 90 Hz. Lower three v–i plots are measured data for 1 V peak input sine at: (d) 10 Hz, (e) 30 Hz, and (f) 90 Hz, with 1.5 V dc offset due to unipolar ADC and DAC.

$G(\varphi[n]) = K_G/\varphi[n]$, and the input current becomes $i[n] = (v[n] - v_{dac}[n])/R_{dac} = v[n]\,K_G/\varphi[n]$. Rearranging, the discrete-time formulation of the proposed memristor in (1) and (2) for Fig. 1 becomes

$$i[n] = v[n]\,G(\varphi) = K_G\frac{v[n]}{\varphi[n]} \tag{3}$$

$$\varphi[n] = \varphi_\circ + T_c\sum_{\alpha=1}^{n} v[\alpha] \quad \forall \quad n > 1 \tag{4}$$

$$v_{dac}[n] = v[n]\left(1 - \frac{R_{dac}K_G}{\varphi[n]}\right) \tag{5}$$

where $n \geq 0$, $\varphi[0] = \varphi_\circ$, and at each step $R[n] = 1/G[n] = \varphi[n]/K_G = v[n]/i[n]$ is the large-signal chord memristance, as defined in [3].

To provide insight and evaluate results, it is useful to compute the theoretical current, i_{vp}, when the sinusoidal input voltage is at its peak. A second useful parameter is the overall peak current, i_p, during a full cycle of $v(t)$. To derive these parameters, first let $R_{min} = R[0] = \varphi_\circ/K_G$ be the minimum large-signal chord memristance. From the integral in (2), the peak-to-peak flux for a zero-mean sinusoidal input $v(t)$ with peak voltage V_p and signal frequency f_s is $\varphi_{pp} = V_p/(\pi f_s)$. The maximum flux is then $\varphi_\circ + V_p/(\pi f_s)$, leading to a maximum large-signal chord memristance of $R_{max} = 1/G_{min} = \{\varphi_\circ + V_p/(\pi f_s)\}/K_G$. At the time instant of peak voltage for sinusoidal $v(t)$, the integral of half of the positive cycle of $v(t)$ yields half of the maximum flux change, and thus the theoretical current at the peak input voltage is

$$i_{vp} = V_p/\left(R_{min} + 0.5\,R_\Delta\right)\,, \tag{6}$$

where $R_{max} = R_{min} + R_\Delta$, and $R_\Delta = V_p/(\pi f_s K_G)$ is the maximum change in resistance over one cycle. Similarly, overall peak current i_p can by computed by assuming $v(t) = \sin(2\pi f_s t)$ and noting that at $t = 0$ the flux and large-signal chord memristance $R(t)$ are minimum. Then, $R(t)$ must equal R_{min} at $t = 0$, so $R(t) = R_{min} + \{1 - \cos(2\pi f_s t)\}R_\Delta/2$, and the current must be $i(t) = v(t)/R(t) = 2\sin(2\pi f_s t)/\left[2R_{min} + \{1 - \cos(2\pi f_s t)\}\,R_\Delta\right]$. Taking the derivative and setting it equal to zero to find the maximum current during a full cycle of $v(t)$ yields

$$i_p = 2\sin(\theta)/[2R_{min} + \{1 - \cos(\theta)\}R_\Delta]\,, \tag{7}$$

where $\theta = \cos^{-1}(R_\Delta/\{2R_{min} + R_\Delta\})$.

Lastly, changes in clock frequency can be best understood by recalling that (4) is a discrete-time approximation to the integral in (2) for clock frequency $f_c = 1/T_c$. If the initial external clock frequency is f_{ca}, and is then changed to a different clock frequency $f_{cb} = 1/T_{cb}$, the flux becomes improperly computed as $\varphi_b[n] = \varphi_\circ + T_{ca}\sum\sin(n2\pi f_{sb}T_{cb})$ instead of $\varphi_b[n] = \varphi_\circ + T_{cb}\sum\sin(n2\pi f_{sb}T_{cb})$. In addition, if the initial signal frequency of $v(t)$ is f_{sa}, and it is changed to a different signal frequency f_{sb}, then the overall peak-to-peak resistance changes from $R_{\Delta a}$ to $R_{\Delta b}$ as

$$R_{\Delta a} = V_p/(\pi f_{sa}K_G) \tag{8}$$

$$R_{\Delta b} = f_{cb}V_p/(f_{ca}\pi f_{sb}K_G)\,, \tag{9}$$

where it can be observed that $R_{\Delta b} = R_{\Delta a}$ if $f_{sa} = f_{sb}f_{ca}/f_{cb}$ or if $f_{sb} = f_{sa}f_{cb}/f_{ca}$. *Therefore, setting a clock frequency of $f_{cb} = f_{sb}f_{ca}/f_{sa}$ produces the same memristor behavior at input frequency f_{sb} as was originally obtained for input frequency f_{sa} with clock f_{ca}.* This forms the basis for the proposed clock tuning.

III. Simulations and Prototype Measurements

The simulation results in Figs. 2(a)–(c) were generated using the relations in (1) and (2) with Mathcad software, for comparison to the measured prototype data shown in Figs. 2(d)–(f).

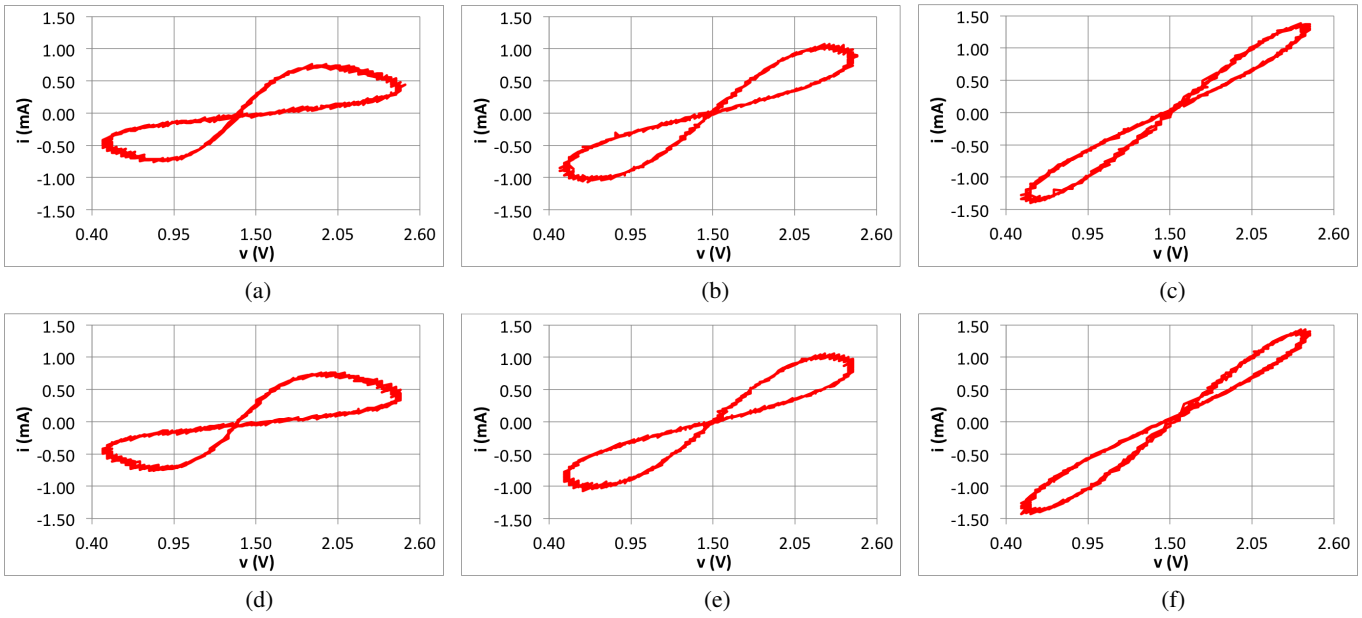

Fig. 3. Measured pinched hysteresis loops with clock frequency varied by factor of 100:1. Upper three plots are for a ***500 Hz clock*** and show measured pinched hysteresis loop v–i plots for 1 V peak input sine wave at: (a) 1 Hz, (b) 3 Hz, and (c) 9 Hz, with 1.5 V dc offset due to unipolar ADC and DAC. Lower three plots are for a ***50 kHz clock*** and show measured v–i plots for 1 V peak input sine wave at: (d) 100 Hz, (e) 300 Hz, and (f) 900 Hz, with 1.5 V dc offset due to unipolar ADC and DAC. ***Thus, the operating frequency band shifts by a factor of 100:1***.

An NXP FRDM-K64F development board was used to implement the prototype of the system of Fig. 1, with embedded software to compute (3), (4), and (5). Based on the capabilities of the FRDM-K64F board with $R_{dac} = 1000$ ohms, the baseline clock frequency of the MCU signal processing software was $f_{ca} = 1/T_{ca} = 10$ kHz, with $K_G = 4 \times 10^{-6}$, and $\varphi_\circ = 2 \times 10^{-3}$, resulting in $R_{min} = \varphi_\circ / K_G = 500$ ohms.

Figs. 2(a)–(c) show simulation results for clock frequency $f_c = 5$ kHz, and input sinusoids $v(t)$ of 1 V peak at signal frequencies f_s of 10 Hz, 30 Hz, and 90 Hz respectively. All three figures show the pinched hysteresis loop v–i characteristic of a memristor [8]. In Fig. 2(a) with $f_s = 10$ Hz, $R_\Delta = V_p/(K_G \pi f_s f_{ca}/f_c) = 1/(4 \times 10^{-6} \pi \cdot 10 \cdot 10{,}000/5{,}000) = 3979$ ohms, resulting in a current when the voltage is peak of $i_{vp} = V_p/(R_{min} + 0.5\, R_\Delta) = 1/(500 + 0.5 \cdot 3979) = 0.40$ mA, nearly equal to the 0.41 mA from simulation. The predicted overall maximum current during a full cycle of $v(t)$ yields $\theta = \cos^{-1}(R_\Delta/\{2R_{min} + R_\Delta\}) = \cos^{-1}(3979/\{2 \cdot 500 + 3979\}) = 37°$, and $i_p = 2\sin(\theta)/[2R_{min} + \{1 - \cos(\theta)\} R_\Delta] = 1.20/1801 = 0.67$ mA, equal to the 0.67 mA simulated. Similarly for Fig. 2(b), theoretical $R_\Delta = 1326$ ohms, $i_{vp} = 0.86$ mA compares well with the 0.85 mA simulated, and $\theta = 55°$ gives $i_p = 1.04$ mA nearly equals the 1.05 mA simulated. For Fig. 2(c), theoretical $R_\Delta = 442$ ohms, $i_{vp} = 1.39$ mA compares well with the 1.38 mA simulated, and $\theta = 72°$ gives $i_p = 1.46$ mA which equals the 1.46 mA simulated.

Figs. 2(d)–(f) show prototype measurement results for clock frequency $f_c = 5$ kHz, and input sinusoids $v(t)$ of 1 V peak at signal frequencies f_s of 10 Hz, 30 Hz, and 90 Hz respectively. All three figures closely resemble the corresponding simulations directly above in Figs. 2(a)–(c), except for a slight asymmetry and left-shifted "pinch point" in Fig. 2(d). As noted in [9], experimentally-measured pinched hysteresis loops of some "real memristors" may not pass through the origin. In addition, the voltage axes of the measured data are centered at 1.5 V instead of 0 V, because the 16-bit ADC and 12-bit DAC of the development board operate between 0 V and 3.3 V, requiring the ground reference voltage of the MCU signal processing to be set at 1.5 V. Nevertheless, bipolar current is possible, since negative current can be produced when $v(t) < v_{dac}(t)$ in Fig. 1.

Next, the frequency tuning of the memristor prototype was tested for a 100:1 ratio of clock frequencies. Figs. 3(a)–(c) show prototype measurement results for clock frequency $f_c = 500$ Hz, and input sinusoids $v(t)$ of 1 V peak at signal frequencies f_s of 1 Hz, 3 Hz, and 9 Hz respectively. Figs. 3(d)–(f) show prototype measurement results for clock frequency $f_c = 50$ kHz, and input sinusoids $v(t)$ of 1 V peak at signal frequencies f_s of 100 Hz, 300 Hz, and 900 Hz respectively. Clearly, the three plots of Figs. 3(a)–(c) at $f_c = 500$ Hz closely resemble the corresponding three plots directly below in Figs. 3(d)–(f). *Thus, the results of Fig. 3 experimentally confirm effective tuning of the memristor operating frequency band over a range of at least two decades, from a memristor signal frequency band f_s = 1–9 Hz to f_s = 100–900 Hz.* Also, note that Figs. 2(a)–(c) demonstrate the same performance at an intermediate frequency band of $f_s = 10$–90 Hz, for $f_c = 5$ kHz.

Note that for a given clock frequency, the v–i curve is frequency dependent. For example, when the signal frequency is changed from 1 Hz in Fig. 3(a) to 9 Hz in Fig. 3(c), the v–i curve changes significantly. Similarly, when the signal frequency is changed from 100 Hz in Fig. 3(a) to 900 Hz in Fig. 3(c), the v–i curve changes significantly. However, note

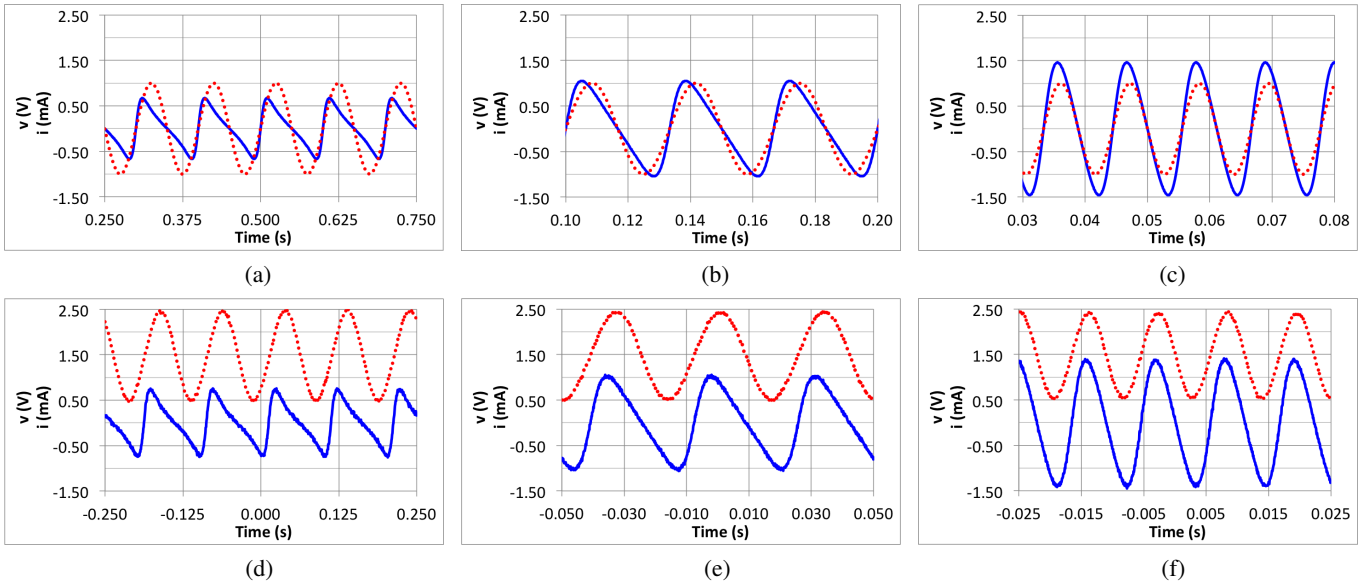

Fig. 4. Simulated and measured time-domain signals with 5 kHz clock. Upper three simulation plots show current $i(t)$ in solid blue and 1 V peak input sine wave $v(t)$ in dotted red at: (a) 10 Hz, (b) 30 Hz, and (c) 90 Hz. Lower three plots are measured data for 1 V peak input sine wave at: (d) 10 Hz, (e) 30 Hz, and (f) 90 Hz, with current $i(t)$ in solid blue and input $v(t)$ in dotted red, with 1.5 V dc offset due to unipolar ADC and DAC.

that by changing the clock from $f_c = 500$ Hz in Figs. 3(a)–(c), to $f_c = 50$ kHz in Figs. 3(d)–(f), the clock-tuning makes it possible to achieve the same v–i curves in the higher frequency range as were obtained in the lower frequency range. *Thus, the operating frequency band can be shifted by a factor of 100:1, by changing the clock frequency f_c by a factor of 100.*

Figs. 4(a)–(c) show time-domain simulation results for clock frequency $f_c = 5$ kHz, and input sinusoids $v(t)$ of 1 V peak at signal frequencies f_s of 10 Hz, 30 Hz, and 90 Hz respectively. These three figures correspond to the pinched hysteresis loop v–i results of Figs. 2(a)–(c). Measured prototype time-domain results are given in Figs. 4(d)–(f) for clock frequency $f_c = 5$ kHz, and input sinusoids $v(t)$ of 1 V peak at signal frequencies f_s of 10 Hz, 30 Hz, and 90 Hz respectively. In all plots of Fig. 4, the dotted red curves are the memristor voltage $v(t)$, and the solid blue curves are the memristor current $i(t)$. The simulation results of Figs. 4(a)–(c) closely resemble the measured results of Figs. 4(d)–(f), except for the dc offset voltage of 1.5 V observed in the measured data arising from the previously mentioned 1.5 V ground reference voltage of the MCU required for the ADC and DAC single-ended operating voltage ranges. Lastly, the prototype is shown in Fig. 5, and only requires a single external component, R_{dac}, and connection to the external clock port "clk" of Fig. 1.

IV. Conclusion

A clock-tuned digital memristor has been demonstrated with 100:1 change in operating frequency band. In particular, the measured v–i curve for a 1 V peak input signal at 3 Hz with 500 Hz clock was shown to be nearly identical to the v–i curve for a 1 V peak input signal at 300 Hz with the clock changed to 50 kHz. Although the embedded software implementation of (3), (4), and (5) is straightforward, practical considerations should also be noted. First, the clock-tuned feature is implemented by the MCU waiting for a low-to-high clock transition. Second, the clock frequency f_c should be much higher than the signal frequency. Third, the MCU computation plus ADC and DAC conversions must complete within one clock cycle. Fourth, flux φ error due to dc offsets and drift are avoided by MCU continually monitoring dc average input, correcting drift, and setting initial flux (in software) at startup. Fifth, the embedded software approach is quite general and offers the potential to emulate other non-ideal memristor characteristics noted in [9]. Such practical details tend to be application specific, but are included here to provide general insights for future applications. Further, a floating two-terminal version should be possible on a microcontroller with a differential ADC and DAC. Lastly, the clock-tuned memristor may inspire investigators to discover new clocked memristors or "clock-pumped memristors" similar to pumped varactors.

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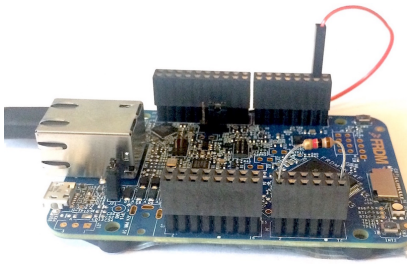

Fig. 5. Prototype of clock-tuned memristor with resistor R_{dac} installed on terminal strip in foreground, and red wire at top of figure on terminal strip in background connecting to clock signal.

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