Performance of Digital Discrete-Time Implementations of Non-Foster Circuit Elements

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***Abstract*—There is renewed interest in the use of non-Foster circuit elements in a variety of important applications such as wideband impedance matching and artificial magnetic conductors. Although non-Foster devices such as negative capacitors and negative inductors can be realized using current conveyors and Linvill circuits, a digital design approach may offer an important alternative in some applications. Therefore, digital discrete-time implementations of non-Foster circuit elements are investigated, and simulation results are presented for the implementation of a discrete-time negative inductor and a discrete-time negative capacitor.**

I. Introduction

Recently, there has been a resurgence of interest in the use of non-Foster circuit elements to improve system performance and bandwidth in a variety of applications such as impedance matching networks, electrically small antennas, metamaterials, and magnetic conductors [1]–[4]. In such applications, non-Foster elements such as negative capacitors and negative inductors are commonly realized using analog approaches such as Linvill circuits and current conveyors [1], [5]–[7]. Although such analog non-Foster circuits are well established, a digital design approach may be advantageous in some applications.

Therefore, digital discrete-time implementations of non-Foster circuit elements are considered [8]. In this digital approach, the analog voltage at the input terminals is first digitized with an ADC (analog-to-digital converter). The behavior of the circuit is then established through digital signal processing that determines the appropriate current for the measured voltage. Finally, the current at the input terminals is established by a current-output DAC (digital-to-analog converter). Such a digital implementation offers the potential for well-controlled circuit performance that is governed by the underlying digital signal processing. In addition, digital implementation offers potential for adaptive algorithms in complex systems and for uniformity in systems such as metamaterials and arrays comprised of many elements.

In the following section, the general approach and underlying analysis is first described. In the two subsequent sections, simulation results are given for example implementations of a discrete-time negative capacitor and a discrete-time negative inductor.

II. Digital non-Foster Circuit Elements

A block diagram of a digital discrete-time implementation of a non-Foster circuit element is shown in Fig. 1. In this, a continuous-time analog input voltage $v(t)$ is first digitized by an ADC with clock period T to produce discrete-time output $v[n]$. For the purposes of the present discussion, $v[n]$ undergoes signal processing in block $H(z)$ to form the discrete-time current output $i[n] = v[n] * h[n]$, where $*$ denotes convolution, $H(z)$ is the z-transform of $h[n]$, and $I(z) = H(z)V(z)$. In other applications such as adaptive systems, the signal processing $H(z)$ can be more complicated than simple convolution.

In the final stage of Fig. 1, discrete-time current $i[n]$ is converted into continuous-time current $i(t)$ by the current-output DAC with clock period T, most commonly with ZOH (zero-order hold) incorporated. Here, the input impedance of the ADC and the output impedance of the DAC are assumed to be infinite, for simplicity in the present analysis. Note also that the concept illustrated in Fig. 1 can be applied to balanced circuit elements, or to single-ended circuit elements with one terminal grounded. The Laplace transform of input current $i(t)$ is then

$$I(s) = V^\star(s)\frac{H(z)(1-z^{-1})}{s}\bigg|_{z=e^{sT}} = \sum_{m=-\infty}^{\infty} \frac{V(s-j2m\pi/T)}{T}\frac{H(z)(1-z^{-1})}{s}\bigg|_{z=e^{sT}}, \quad (1)$$

correction

for integer m, and where $V^\star(s) = \sum v(nT)e^{-nsT}$ for integer n is the starred transform [9]. For signals sampled without aliasing, the input impedance of Fig. 1 below the Nyquist

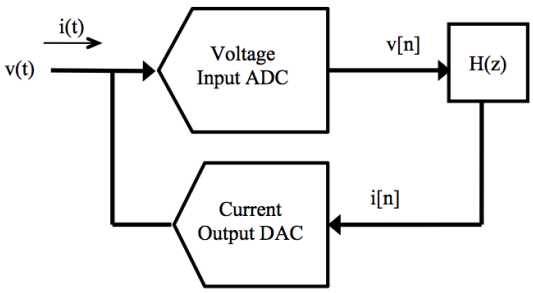

Fig. 1. Block diagram of digital discrete-time non-Foster circuit. Continuous-time input voltage $v(t)$ is digitized by the ADC into discrete-time signal $v[n]$, then processed by a discrete-time filter with z-transform $H(z)$ to form discrete-time current $i[n]$, which is finally converted into continuous-time input current $i(t)$ by the DAC. As illustrated, the ADC and DAC would have high impedance, $I(z) = H(z)V(z)$, $v[n] = v(nT)$ and $i[n] = i(nT)$ for integer n and clock period T.

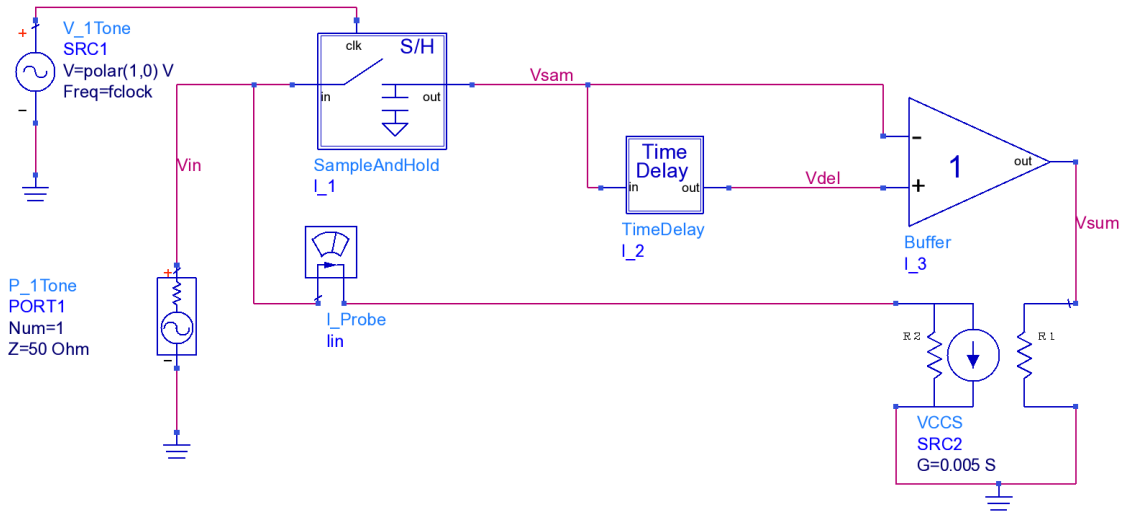

Fig. 2. Schematic in Keysight ADS simulator of a -25 pF discrete-time negative capacitor, with $H_C(z) = C(1-z^{-1})/T = -0.005(1-z^{-1})$. Source SRC1 is the system clock and sets the sample period at T, and 50 Ω input source PORT1 generates the input signal V_{in} which is sampled by sample-and-hold circuit I_1 to generate sampled signal V_{sam}. The output V_{del} of delay line I_2 corresponds to $v[n-1]$, and the output of differential buffer amplifier I_3 produces $-(V_{sam} - V_{del})$ corresponding to $-(v[n] - v[n-1])$ with z-transform $-V(z)(1-z^{-1})$. Voltage-controlled current source SRC2 generates the current I_{in} seen by input terminal at PORT1 and monitored by current probe I_probe.

frequency becomes

$$Z(s) = \frac{V(s)}{I(s)} \approx \left.\frac{sT}{[(1-z^{-1})H(z)]}\right|_{z=e^{sT}} \tag{2}$$

for frequencies below $0.5/T$ Hz, assuming a ZOH incorporated into the DAC.

III. A Discrete-Time Negative Capacitor

For the purpose of illustrating the implementation of a non-Foster circuit element using the approach of Fig. 1, a discrete-time negative capacitor is first designed [8]. Since a capacitor has $i(t) = Cdv(t)/dt$, a positive or negative capacitor may be approximated by using the discrete-time backward-difference approximation of the derivative $dv(t)/dt \approx (v[n]-v[n-1])/T$. Using this approximation, the discrete-time current becomes $i[n] = C(v[n] - v[n-1])/T$. Taking the z-transform, this becomes $I(z) = C(1-z^{-1})V(z)/T$. Comparing this to $I(z) = H(z)V(z)$ in Fig. 1, and denoting $H(z)$ for this capacitor as $H_C(z)$, the required transfer function becomes

$$H_C(z) = \frac{C(1-z^{-1})}{T}\,, \tag{3}$$

where T is the ADC and DAC clock period, and C is the desired capacitance. Also, note that C in (3) can be either positive or negative. Thus, the overall input impedance $Z(s)$ from (2) and denoted $Z_C(s)$ for the capacitor is

$$\begin{aligned} Z_C(s) &= \left.\frac{sT}{[(1-z^{-1})H_C(z)]}\right|_{z=e^{sT}} \\ &= \left.\frac{sT^2}{C(1-z^{-1})^2}\right|_{z=e^{sT}} \approx \frac{1}{sC}\,, \end{aligned} \tag{4}$$

for frequencies below $0.5/T$ Hz, and assuming a ZOH incorporated into the DAC.

Fig. 2 shows a schematic diagram of an implementation of a discrete-time negative capacitor using the Keysight ADS simulator. For simplicity and to make use of the ADS large-signal S-parameter simulation to obtain the system input impedance, the quantizer is omitted and analog samplers and delay lines are used in simulating the digital filter. Thus, 50 Ω input source PORT1 generates the input signal V_{in} which is sampled by sample-and-hold circuit I_1 to generate sampled signal V_{sam}. As seen in Fig. 3, V_{sam} is the expected zero-order-hold sampled version $v[n]$ of the input signal V_{in}. Then the delayed signal V_{del} in Fig. 2 representing $v[n-1]$ is generated by delay line I_2, with V_{del} also shown in Fig. 3. Then, V_{sum}

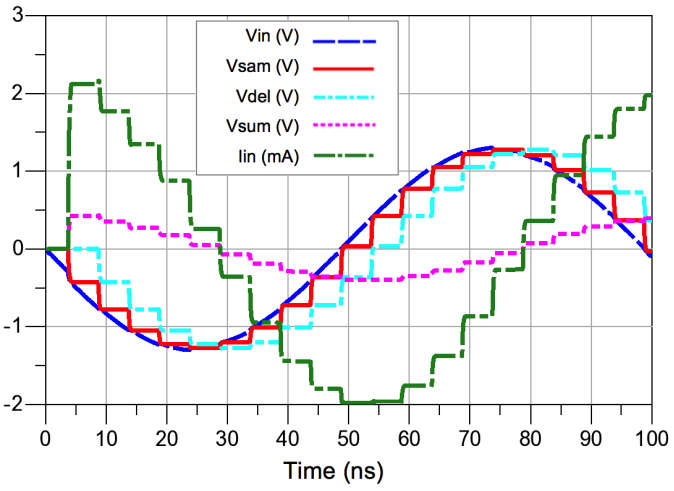

Fig. 3. Keysight ADS transient simulation for Fig. 2 with 10 MHz input at PORT1 and clock period $T = 5$ ns. Signals of Fig. 2 shown include: input signal V_{in}, sample-and-hold output signal V_{sam} corresponding to $v[n]$, V_{del} corresponding to $v[n-1]$, V_{sum} corresponding to $-(v[n] - v[n-1])$, and I_{in} in mA corresponding to $i[n]$ and zero-order-hold DAC output $i(t)$ of Fig. 1.

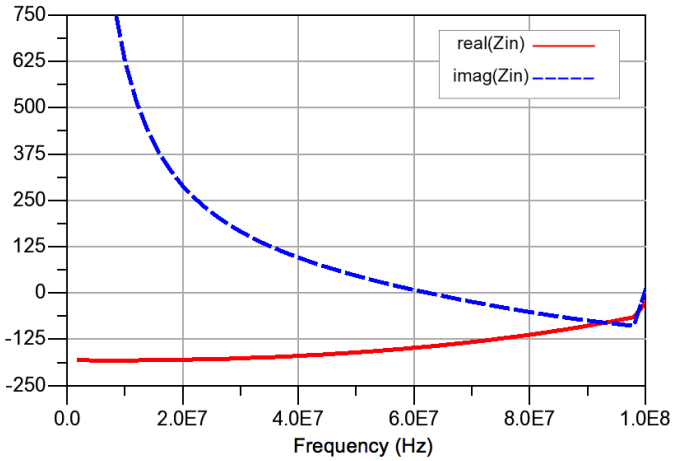

Fig. 4. Keysight ADS large-signal S-parameter simulation results for Fig. 2 with $T = 5$ ns and design target $C = -25$ pF. The solid red curve is the real part of input impedance $Z_C(s)$, and dashed blue curve is the imaginary part of the input impedance $Z_C(s)$, as a function of sinusoidal input frequency in Hz. The predicted impedance is $+j637$ ohms for -25 pF at 10 MHz, and the observed impedance is $-182 + j623$ ohms at 10 MHz.

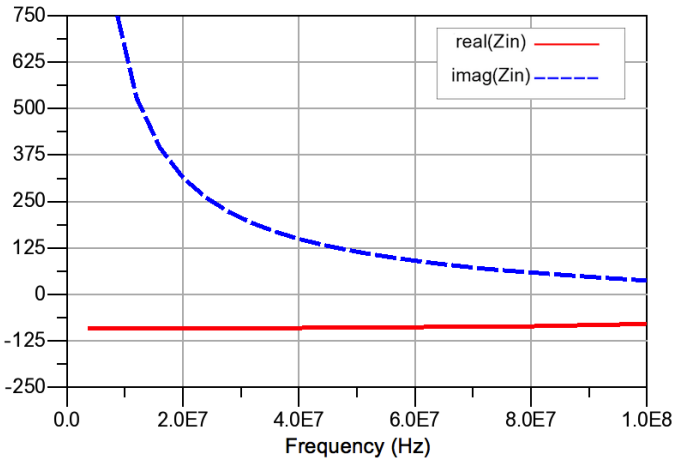

Fig. 5. Keysight ADS large-signal S-parameter simulation results for Fig. 2 with $T = 2.5$ ns and design target $C = -25$ pF. The solid red curve is the real part of input impedance $Z_C(s)$, and dashed blue curve is the imaginary part of the input impedance $Z_C(s)$. As predicted, the observed impedance of $-91 + j529$ ohms at 10 MHz shows that the low-frequency resistance is decreased by half when compared to results of Fig 4.

at the output of the differential unity gain buffer amplifier I_3 produces $-(V_{sam} - V_{del})$ and represents $-(v[n] - v[n-1])$ or $-V(z)(1 - z^{-1})$. Voltage controlled current source SRC2 with transconductance 0.005 S generates the current I_{in} of Fig. 3 as seen at the input terminals and monitored by current probe I_probe in Fig. 2. Source SRC1 is the system clock and sets the sample period at $T = 5$ ns. Thus, the overall transfer function $H_C(s)$ for Fig. 2 is $H_C(z) = C(1 - z^{-1})/T = -0.005(1 - z^{-1})$, and so $C = -25$ pF. Note that the digital functionality of Fig. 1 can also be implemented using analog samplers and delay lines as illustrated in Fig. 2.

Fig. 4 shows simulation results for Fig. 2 with $T = 5$ ns and design target $C = -25$ pF. The solid red curve is the real part of input impedance $Z_C(s)$, and dashed blue curve is the imaginary part of the input impedance $Z_C(s)$. The predicted impedance is $+j637$ ohms for -25 pF at 10 MHz, and the observed impedance is $-182 + j623$ ohms at 10 MHz, or -25.6 pF in series with -182 ohms. In addition, the shape of the reactance approximately follows the expected inverse frequency dependence of $Im[Z(j\omega)] = +1/(\omega|C|)$ for a negative capacitor. In this example, the reactance changes sign beyond 60 MHz, and ceases being a positive reactance. The anomalous impedance and abrupt change at 100 MHz is at the Nyquist frequency $0.5/T$, where the sampling theorem is not satisfied.

The observed real part of $Z_C(s)$ follows from (4) where $Z_C(s) = sT^2/[C(1 - z^{-1})^2] = sT^2 z/[C(1 - z^{-1})(z - 1)] \approx e^{sT}/(sC)$, and upon substituting $z = e^{sT} \approx 1 + sT$, yields $Z_C(s) \approx e^{sT}/(sC) \approx 1/(sC) + T/C$. Thus, the predicted impedance at 10 MHz including the resistive component T/C is approximately $-200 + j637$ ohms, in good agreement with the observed impedance. For the same -25 pF capacitance, this resistance can be lowered by changing the transconductance of SRC2 to 0.01 S and decreasing the clock period to $T = 2.5$ ns. For this modified design, the predicted resistance should decrease by half for -25 pF at 10 MHz, and this reduced resistance is observed in the impedance of Fig. 5 with $-91 + j529$ ohms at 10 MHz.

IV. A Discrete-Time Negative Inductor

Using the approach of Fig. 1, an example of a discrete-time negative inductor design can also be considered [8]. Since an inductor has a current $i(t) = i(0) + \int v(t)dt/L$, it may be approximated using the discrete-time accumulator approximation to the integral $i(0) + \int v(t)dt/L \approx i[0] + \sum v[n]T/L$, and setting $i[n] = i[n-1] + Tv[n]/L$. Taking the z-transform, the inductor current is $I(z) = TV(z)/(L - z^{-1}L)$. Denoting $H(z)$ for this inductor as $H_L(z)$, the transfer function becomes

$$H_L(z) = \frac{T}{L(1 - z^{-1})}, \tag{5}$$

where T is the ADC and DAC clock period, and L is the desired inductance. Also, note that L in (5) can be either positive or negative. Thus, the overall input impedance $Z(s)$, denoted $Z_L(s)$, is

$$Z_L(s) = \left.\frac{sT}{[(1 - z^{-1})H_L(z)]}\right|_{z=e^{sT}} \approx sL, \tag{6}$$

for frequencies below $0.5/T$ Hz, and assuming ZOH incorporated into the DAC. Alternatively, a positive or negative inductor could be approximated by using the bilinear transform approximation of the relation $I(s) = V(s)/(sL)$, replacing s by $2(z - 1)/[(z + 1)T]$ and then yielding $I(z) = TV(z)(z+1)/[2L(z-1)]$, so $H_L(z) = T(z+1)/[2L(z-1)]$ in this case [8]. Similarly, the bilinear transform could be used in the design of the capacitor.

Fig. 6 shows a schematic diagram of an implementation of a discrete-time negative inductor using the Keysight ADS simulator, along the same lines as Fig. 2. Fig. 7 shows simulation results for Fig. 6 with $T = 5$ ns and design target $L = -1$ μH. The solid red curve is the real part of input impedance $Z_L(s)$, and dashed blue curve is the imaginary part of the input impedance $Z_L(s)$. The predicted impedance

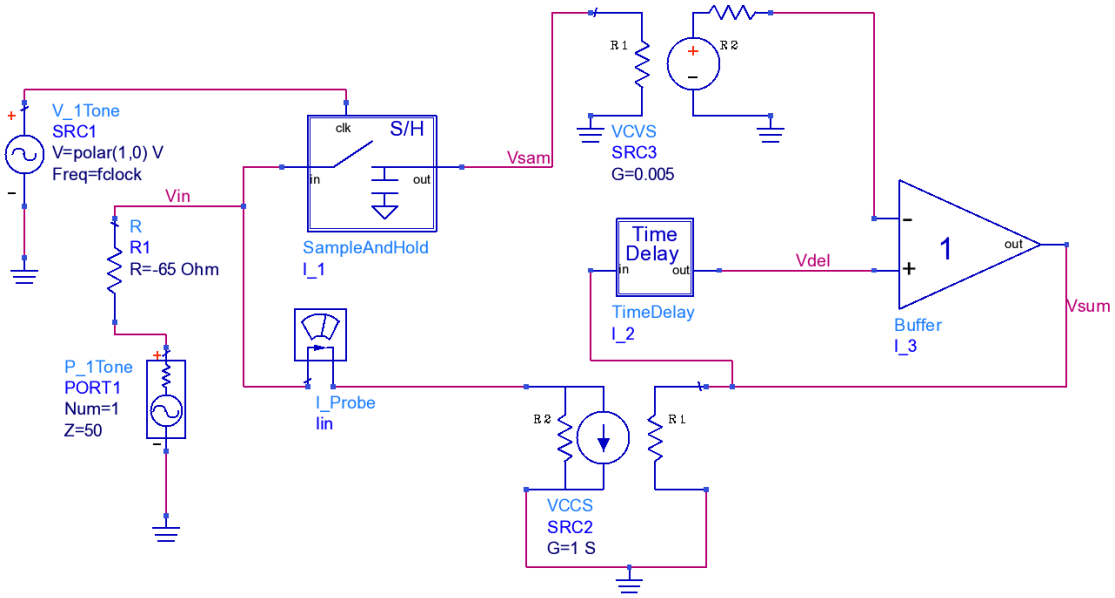

Fig. 6. Schematic in ADS simulator of a -1 μH discrete-time negative inductor, with $i[n] = i[n-1] + Tv[n]/L = i[n-1] - 0.005v[n]$ and $H_L(z) = T/[L(1-z^{-1})]$. Source SRC1 is the system clock and sets the sample period at T, and 50 Ω input source PORT1 generates the input (-65 Ω resistor R1 is used for stabilization, but later subtracted from results in Fig. 7). Signal V_{in} is sampled by sample-and-hold circuit I_1 to generate sampled signal V_{sam}. SRC3 multiplies V_{sam} by 0.005. The output V_{del} of delay line I_2 corresponds to $i[n-1]$, and the output of differential buffer amplifier I_3 produces $V_{del} - 0.005V_{sam}$ corresponding to $i[n-1] - 0.005v[n]$. Voltage controlled current source SRC2 generates the current I_{in} seen by input terminal at PORT1 and monitored by current probe I_probe.

is $-j62.8$ ohms for -1 μH at 10 MHz, and the observed impedance is $-3.5 - j70$ ohms at 10 MHz, or -1.1 μH in series with -3.5 ohms.

V. Conclusion

The analysis for a general approach to implement digital discrete-time non-Foster circuit elements was presented. Using this approach, results have been presented for a discrete-time negative inductor and a discrete-time negative capacitor that are in good agreement with the analysis. In addition, a design technique to reduce the resistive component of the impedance was presented.

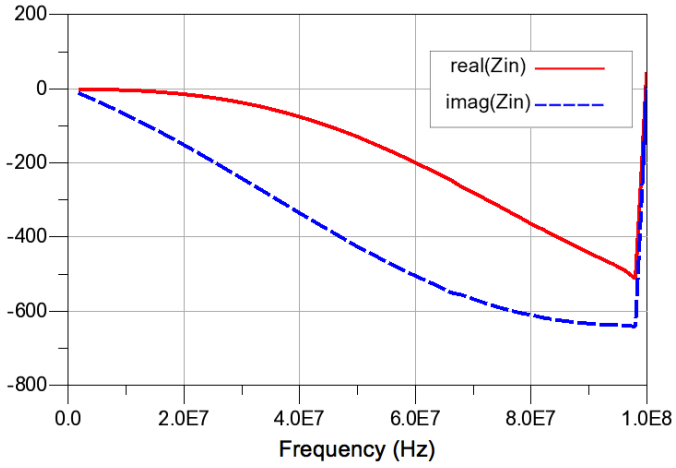

Fig. 7. Keysight ADS large-signal S-parameter simulation results for Fig. 6 with $T = 5$ ns and design target $L = -1$ μH. The solid red curve is the real part of the input impedance $Z_L(s)$, and the dashed blue curve is the imaginary part of the input impedance $Z_L(s)$, as a function of sinusoidal input frequency in Hz. The predicted impedance is $-j62.8$ ohms for -1 μH at 10 MHz, and the observed impedance is $-3.5 - j70$ ohms at 10 MHz, or -1.1 μH in series with -3.5 ohms.

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