Experimental Results at One GHz on Linearizing an NMOS Transistor with a Parallel PMOS Transistor

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***Abstract* — A simple circuit consisting of an nMOS transistor in parallel with a pMOS transistor is shown to reduce nonlinear distortion. Measured experimental results show more than 10 dB reduction in third order distortion at 1 GHz for a prototype 0.18 micron CMOS integrated circuit. Experimental data further suggest that the relative increase in third order output intercept point greatly exceeds the corresponding increase in power supply current. Since the proposed circuit is itself a three-terminal device, it can also be used as a building block for larger circuits. Finally, theoretical linearization conditions are presented in terms of the gains and intercept points of the nMOS and pMOS devices.**

***Index Terms* — Amplifier distortion, distortion, feedforward amplifiers, nonlinear circuits, nonlinearities.**

I. Introduction

In earlier results, linearization conditions were presented for a simple feedforward topology comprised of two amplifier stages with equal-amplitude couplers [1]-[2]. In this, a simple equation relating the gains and intercept points of the amplifiers was used to define the linearization conditions.

The present paper focuses on an extremely simple circuit consisting of a single nMOS transistor in parallel with a single pMOS transistor. The composite device behaves as a new three-terminal transistor with improved linearity, and is based on the earlier topology in [1]-[2].

Beyond the proposed circuit, the underlying design approach provides insight for the development of alternative circuit configurations. For example, the nMOS and pMOS devices could be replaced with NPN and PNP BJT transistors or combinations of BJT and FET transistors.

Other researchers have presented more complex linearization methods including feedforward [3]-[4], Envelope Elimination and Restoration (EER) [3], Linear Amplification Using Nonlinear Components (LINC) [5], Digital Predistortion [6], and others [7]-[9]. Each of these earlier techniques have advantages and disadvantages in cost, complexity, signal processing overhead, component phase or time delay matching, and the like. In integrated circuit applications, cross-coupled amplifiers have been investigated [10]-[12]. Results in [1] include cross-coupled differential pair linearization conditions in terms of intercept points and gains of amplifiers.

More recently, Otaka et al. [13] demonstrated a direct-conversion mixer following the general linearization methods that were given in the earlier paper [1] and given in Fig. 3, Fig. 4, and claim 14 of the earlier patent [2]. Similarly, Yum et al. [14] presented a BJT-based implementation, the year after the earlier paper [1].

In the following, the fundamental design approach is first presented using device intercept points and a spectral viewpoint. In this, nonlinear components of frequency spectra are considered throughout the system and cancelled at the final output. Linearization conditions are first given for a two stage topology consisting of a single nMOS transistor in parallel with a single pMOS transistor. Then, measured data is given for a prototype integrated circuit using a TSMC 0.18 micron CMOS process. Finally, a four-stage approach is proposed.

II. Two-Stage Linearization Conditions

In earlier work, results were presented for a two-stage linearization topology where the input signal was split equally between both stages [1]. A similar two-stage linearization topology is shown in Fig. 1, except with variable input and output coupling [2]. The input signal P_{in} is first split into two signals P_{1i} and P_{2i} by coupler C_1. The outputs of the coupler are then applied to the inputs of the two nonlinear devices, D_1 and D_2. Typically, these two nonlinear devices would be amplifiers, but they could also be other devices such as mixers, etc. Finally, the outputs of the nonlinear devices, signals P_{1o} and P_{2o}, are recombined in output coupler C_2 to form the final output, P_{out}. In most cases, either the input or output coupler includes a 180 degree relative phase shift such that the undesired nonlinearities are cancelled in the output.

If a two-tone input is applied to each of the two nonlinear devices, D_1 and D_2, the output spectra may appear as illustrated in Fig. 1(a)-(c). In each spectrum, the two innermost spectral lines represent the two original input frequencies, and the two outermost spectral lines in each spectrum represent third order distortion products.

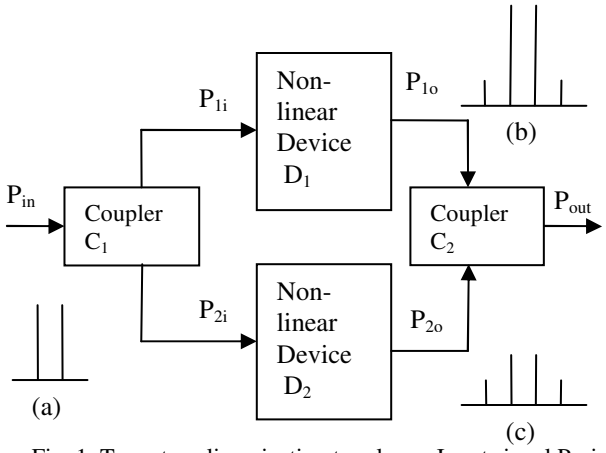

Fig. 1. Two-stage linearization topology. Input signal P_{in} is split into two signals, P_{1i} and P_{2i} , that are inputs to nonlinear devices D_1 and D_2 (typically amplifiers). The output signals from the nonlinear devices, P_{1o} and P_{2o}, are recombined in coupler C_2 to form the final output signal P_{out}. Illustration of frequency spectra at: (a) Pin, (b) P_{1o} , and (c) P_{2o} where two outermost spectral lines in spectrum (b) and (c) represent third order distortion products.

The third-order two-tone intermodulation distortion for each nonlinear device may be calculated as

$$P3 = OIP3 - 3\left(OIP3 - P_{out}\right), \qquad (1)$$

where P_{out} is the linear output power level in dBm, P3 is the output power level of the third order distortion in dBm, and OIP3 is the output third order intercept point of the device in dBm. Using these definitions, the third order output distortion level of nonlinear device D_1 is

$$P3_1 = OIP3_1 - 3\left(OIP3_1 - (P_{1i} + G_1)\right), \qquad (2)$$

where $P3_1$ is the output power level of the third order distortion in dBm for device D_1, and where $OIP3_1$ and G_1 are the output intercept point and gain of D_1. For simplicity, define the coupling coefficient of coupler C_1 as $K_1 = P_{2i} - P_{1i}$ where K_1 is in dB and P_{1i} and P_{2i} are in dBm. Since $P_{2i} = P_{1i} + K_1$, the third order output distortion level of nonlinear device D_2 is

$$P3_2 = OIP3_2 - 3\left(OIP3_2 - (P_{1i} + K_1 + G_2)\right), \qquad (3)$$

where $P3_2$ is the output power level of the third order distortion in dBm for device D_2 and where $OIP3_2$ and G_2 are the output intercept point and gain of D_2.

Finally, let the output coupler combine signals P_{1o} and P_{2o} 180 degrees out of phase. For simplicity, let K_2 define the coupling coefficient of coupler C_2 in relative terms, where the output signal of C_2 in dBm due to signal P_{2o} is equal to $P_{2o}+K_2$, and where the output signal of C_2 due to signal P_{1o} is equal to P_{1o}. Then, the conditions for cancellation of the third order distortion are simply that the power levels of the distortion are equal at the final output P_{out}. Taking into account the coupling coefficient of output coupler C_2, this condition for cancellation of third order distortion is equivalent to $P3_2+K_2=P3_1$. Substituting from Eqs. (2) and (3), third order nonlinearity is cancelled at the output P_{out} in Fig. 1 when

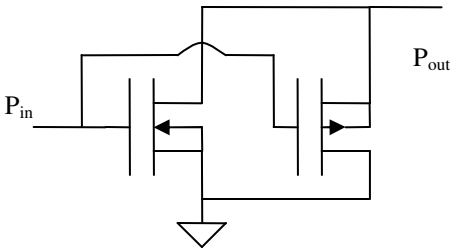

Fig.2. Proposed linearization circuit consisting of an nMOS transistor in parallel with a pMOS transistor.

$$3\left(G_1 - G_2 - K_1 - K_2\right) = 2\left(OIP3_1 - OIP3_2 - K_2\right)) \qquad (4)$$

and where $G_1 \neq G_2 + K_1 + K_2$, so that the linear signal is not cancelled along with the nonlinear distortion. To reduce any signal loss, set $G_1 >> G_2 + K_1 + K_2$.

It is straightforward to extend the results to other order nonlinearities by following the same approach, except that Eq. (1) is replaced by the corresponding equation for the desired order nonlinearity. A detailed analysis for other nonlinearities is found in the patent [2].

To illustrate linearization conditions satisfying Eq. (4), consider the particular case of G_1=13 dB and $OIP3_1$=20 dBm, G_2=5 dB and $OIP3_2$=5 dBm, and K_1= -1 dB and K_2= -3 dB. Next, let the input signal to amplifier D_1 be -10 dBm, which also results in an input to amplifier D_2 of -10 + K_1 = -11 dBm. The third order distortion level at the output of amplifier D_1 becomes 20-3(20-(-10+13))= -31 dBm. Similarly, the third order distortion level at the output of the amplifier D_2 is 5-3(5-(-11+5))= -28 dBm. After the output coupling coefficient K_2, the final output level from D_2 becomes -28+K_2= -31 dBm. Then, the distortion power level at the output is the same for both amplifier stages in this example. Thus, the distortion will be canceled when added 180 degrees out of phase in the second coupler C_2. In addition, the linear signal output levels of the two amplifiers will be -10+G_1= 3 dBm for the first stage and -10+K_1+K_2+G_2= -9 dBm for the second stage. Since the linear components of the signal are of unequal amplitude, they will not be canceled when added 180-degrees out of phase in the output coupler C_2. Furthermore, the cancellation of the nonlinear distortion is

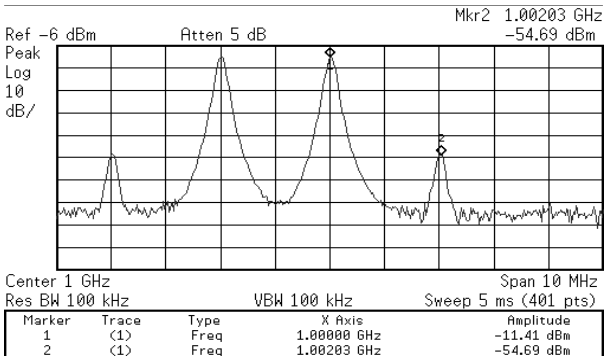

Fig.3. Measured data: Pout for nMOS stage only. Linear tones at -11.4 dBm, third order distortion at -54.7 dBm.

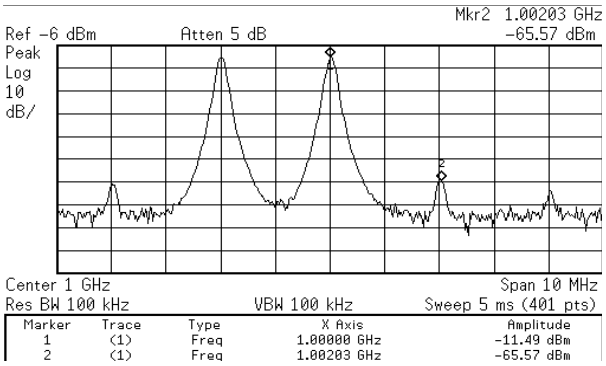

Fig.4. Measured data: Pout for both stages enabled, nMOS and pMOS. Linear tones at -11.5 dBm, third order distortion at -65.6 dBm.

not affected by input signal level, since the third order distortion output of both stages will change 3 dB for each dB change in the linear input signal.

The analysis of Fig. 1 motivates the embodiment shown in Fig. 2, comprised of an nMOS and pMOS device in parallel. The corresponding coupling coefficients are then $K_1=K_2=0$ dB, where D_1 and D_2 of Fig. 1 represent the nMOS and pMOS devices respectively in Fig. 2. For this case, substituting for K_1 and K_2 in Eq. (4), third order nonlinearity is cancelled when

$$3(G_1 - G_2) = 2(OIP3_1 - OIP3_2). \quad (5)$$

It is straightforward to extend results for other order nonlinearities by replacing Eq. (1) with the corresponding equation. Further details are given in the patent [2].

III. Experimental Results

A prototype of the circuit of Fig. 2 was fabricated in the TSMC 0.18 micron CMOS process using the MOSIS fabrication service (www.mosis.org). Based on simulations using Agilent ADS, the nMOS gate was sized 120×0.18 µm, and the pMOS gate was sized 30×0.18 µm. Although only one size ratio was fabricated, other ratios may provide improved results.

Fig. 3 shows the measured output frequency spectrum for the nMOS stage (pMOS stage off) with the two linear output frequencies (998 and 1000 MHz) at a level of -11.4 dBm, and the two third-order distortion frequencies (996 and 1002 MHz) at a level of -54.7 dBm. After rearranging Eq. (1), the output third order intercept point of the nMOS stage is calculated as $OIP3_N$ = -11.4 + (-11.4 - (-54.7))/2 = 10.3 dBm.

Fig. 4 shows the output frequency spectrum of the two-transistor circuit of Fig. 2, with both the nMOS stage and pMOS stage biased on. For this case, the two linear output frequencies are at a level of -11.5 dBm, and the two third-order distortion frequencies are at a level of -65.6 dBm (after increasing the input level 1 dB to overcome the gain loss due to the 180 degree phase shift of the pMOS signal relative to the nMOS signal). Comparing Fig. 3 to Fig. 4, the distortion is reduced by 10.9 dB. The output third order intercept point with both transistors biased on is $OIP3_{N+P}$ = -11.5 + (-11.5 - (-65.6))/2 = 15.6 dBm.

Thus, the third order output intercept point is improved by 5.3 dB when the pMOS stage is enabled. In the foregoing, the current in the nMOS stage of Fig. 3 is 6.8 mA, and the total current for both stages in Fig. 4 is 8.4 mA. Thus, a 5.3 dB improvement in third order intercept point is accompanied by a 24 percent increase in supply current. If intercept point is taken to be proportional to amplifier power, 5.3 dB would correspond to an expected power increase of a factor of 3.38, or a power increase of 238 percent. With these rough estimates, the improved linearity greatly exceeds the increased power consumption.

In Fig. 4, the gate was biased at 0.75 V, and the output biased at 1.6 V where a minimum in distortion was observed. In Fig. 3, the pMOS stage was disabled by lowering the output voltage to 1.1 V, since a circuit with an equivalent nMOS transistor alone was not available on the fabricated circuit. Nevertheless, simulations using Agilent ADS with MOSIS BSIM parameters for run T49PAG show third order distortion reduced by over 30 dB relative to the case of an nMOS transistor alone. The simulation minimum was at an output bias of 1.7 V, corresponding well with the measured data. Simulations also suggest that the pMOS device may degrade the intercept point by as much as 2.5 dB, with the pMOS biased off. With the difficulty of de-embedding the pMOS device from the nMOS device in the circuit, there is further investigation whether linearization mechanism may

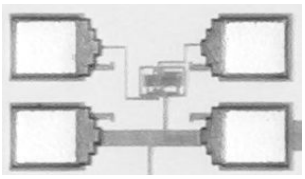

Fig.5. Photograph of chip, showing amplifier of Fig. 2.

be that of Eq. (5), or that of the nonlinear load methods given in Fig. 7 of the patent [2]. Nevertheless, the approach of Fig. 1 motivates the topology of Fig. 2. A photo of the circuit is in Fig. 5. Finally, we note that the circuit of Fig. 2 can linearize other types of circuits, such as class AB circuits.

II. Four-Stage Linearization Conditions

The two-stage topology of Fig. 1 can be extended to the four-stage linearization topology of Fig. 6, similar to a feedforward system with delay lines replaced by amplifiers. In a simplified analysis of Fig. 6, first let the primary signal path be through amplifier A1 and through power amplifier A3, where the output distortion is primarily produced by amplifier A3 with intercept point $OIP3_3$. For an input signal level P_{in} dBm, the output level at A3 is then $P_{in}+G_1+G_3$, where G_1 and G_3 are the gains in dB of A1 and A3. Thus, third order distortion at the output of A3 is approximately $P3_{A3}=OIP3_3-3(OIP3_3-(P_{in}+G_1+G_3))$ dBm. Second, let the signal be nearly cancelled in the lower subtractor, so there is primarily distortion present at the input of A4. Then, $G_2=G_1+K_3$, where K_3 is the attenuator gain in dB. Third, let the dominant distortion component of A4 output be due to the distortion at the output of A2. Then, the third order nonlinear distortion at the output of A4 is approx. $P3_{A4}=G_4+OIP3_2-3(OIP3_2-(P_{in}+G_2))$ dBm. Nonlinearities are then canceled when $P3_{A3}=P3_{A4}$. Substituting, the conditions for linearization become

$$OIP3_3-3(OIP3_3-G_1-G_3)=G_4+OIP3_2-3(OIP3_2-G_2). \quad (6)$$

A more detailed analysis of Fig. 6 is in the patent [2].

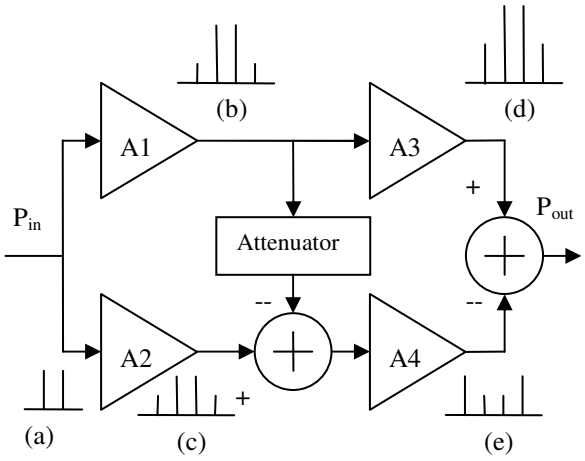

Fig. 6. Four-stage linearization topology.

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