Measurement of a Fast-Wave Line Using Digital Non-Foster Circuits for Software-Adjustable Delay

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***Abstract*—Measured results are compared to simulation results for a wideband software-adjustable fast-wave line using coaxial line sections loaded with digital discrete-time non-Foster circuit elements. In the proposed approach, the negative capacitance of non-Foster circuit elements is varied by changing the signal processing in the digital non-Foster circuit. For the purposes of demonstration and comparison with analog non-Foster approaches, a prototype three-stage fast-wave coaxial line is implemented using three digital negative capacitors. Group delay is shown to be less than in corresponding vacuum propagation, and group delay is shown to be adjustable in software with varied negative capacitance. Measured and simulated results are in good agreement, and closely resemble a frequency-scaled version of prior fast-wave results for analog non-Foster loaded waveguide at higher frequency.**

I. Introduction

Analog non-Foster circuits have been used to design wideband ENZ (epsilon near zero) and fast-wave microstrip for antenna applications [1], [2]. More recently, similar fast-wave transmission lines have been proposed using digital discrete-time non-Foster circuits [3]. In this paper, measured and simulation results are provided to demonstrate a software-adjustable fast-wave line, taking advantage of the inherent digital signal processing in digital non-Foster circuits, and using coaxial line in LF-band for demonstration purposes.

II. Digital Non-Foster Fast-Wave Line

A block diagram of the proposed LF-band non-Foster fast-wave transmission line design is shown in Fig. 1. The approach is similar to the analog non-Foster fast-wave microstrip waveguide in [2], and similar to the digital non-Foster fast-wave approach in [4], except that the present design uses coaxial line sections at lower operating frequency, *and the phase response is digitally adjustable in software by changing the signal processing.* All six of the RG-174 coaxial line sections in Fig. 1 are 15.25 m long, thus comprising three symmetrical tee-sections, with a capacitance C to ground in the middle of each of the three sections, where C is implmented as a negative capacitance with a digital non-Foster circuit.

The block diagram of the digital non-Foster circuit for the negative capacitance is shown in Fig. 2. The input voltage $v_{in}(t)$ of the digital non-Foster circuit element in the dashed box is converted to discrete-time signal $v_{in}[n] = v_{in}(nT)$ by the ADC (analog-to-digital converter) with sampling period T. The digital signal processing denoted by z-transform

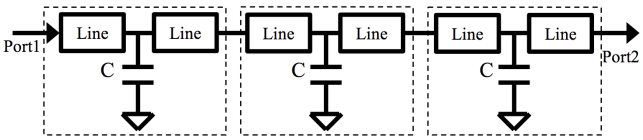

Fig. 1. Block diagram of three-stage fast-wave line, comprised of six coaxial 15.25 m long line sections of RG-174 and three negative capacitors, implemented as digital non-Foster circuit elements with capacitance C.

$H(z)$ forms output $v_{dac}[n]$ where $V_{dac}(z) = V_{in}(z)H(z)$. The DAC (digital-to-analog converter) forms continuous-time output $v_{dac}(t)$, where a ZOH (zero-order hold) is commonly employed. In addition, time delay τ is included to model latency effects caused by ADC and DAC conversion time, and computation time. Finally, external resistors $R_1 = 50\,\Omega$ and $R_2 = 4700\,\Omega$ are added to the circuit of Fig. 2 to empirically stabilize the overall circuit of Fig. 1.

The input current to the dashed box of Fig. 2 is then $i_{in}(t) \approx [v_{in}(t) - v_{dac}(t-\tau)]/R_{dac}$. As will be demonstrated in the following simulation, negative capacitance can be obtained when the signal processing has z-transform

$$H(z) = \left[(T - R_{dac}C)\,z + R_{dac}C\right] / \left(Tz\right) \ . \tag{1}$$

The resulting impedance of the digital non-Foster circuit element $Z(s)$, including latency, can then be shown to be

$$Z(s) \approx \left. \frac{sT\ R_{dac}}{sT - H(z)(1-z^{-1})e^{-s\tau}} \right|_{z=e^{sT}} , \tag{2}$$

where C is the desired capacitance, and for $v_{in}(t)$ sampled without aliasing and at frequencies below $0.5/T$ Hz. The total impedance including R_1 and R_2 is $Z_{tot}(s) = R_1 + R_2||Z(s)$.

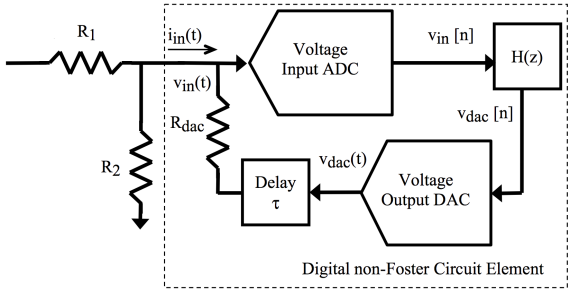

Fig. 2. Block diagram of digital non-Foster circuit element (dashed box), with $R_1 = 50\,\Omega$ and $R_2 = 4700\,\Omega$ added for stabilization. Voltage $v_{in}(t)$ is converted to discrete-time signal $v_{in}[n] = v_{in}(nT)$ by the ADC with sampling period T, and $v_{dac}[n]$ is given by z-transform $V_{dac}(z) = V_{in}(z)H(z)$. DAC output $v_{dac}(t)$ includes latency time delay τ.

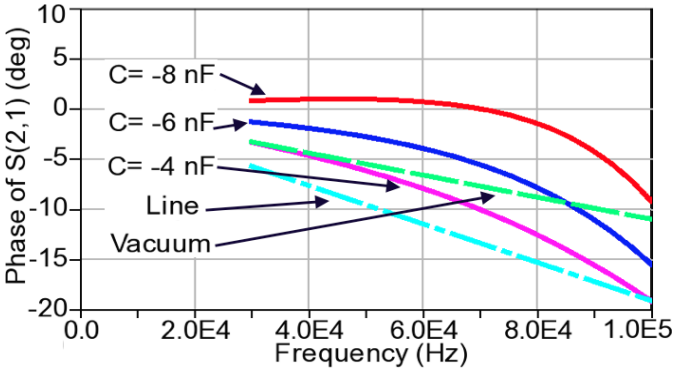

Fig. 3. ADS large-signal S-parameter simulation results for Fig. 1 using Fig. 2 showing phase of S_{21} in degrees for $T = 1\,\mu$s, $R_{dac} = 1000\,\Omega$, $\tau = 1\,\mu$s, $R_1 = 50\,\Omega$, $R_2 = 4700\,\Omega$, six 15.25 m long RG-174 line sections, and $H(z)$ in (1). Solid red curve is for $C = -8$ nF, blue for $C = -6$ nF, and magenta for $C = -4$ nF. Long-dashed green curve is for propagation in vacuum, and dash-dotted cyan is unloaded RG-174 line.

III. Simulation

The system of Fig. 1 using digital negative capacitors of Fig. 2 and (1) was simulated using ADS large-signal S-parameters, as similarly described in [3]. Simulation parameters were $T = 1\,\mu$s, $R_{dac} = 1000\,\Omega$, $R_1 = 50\,\Omega$, $R_2 = 4700\,\Omega$, latency time delay $\tau = 1\,\mu$s, and with values of C varied. Fig. 3 shows the phase of S_{21}, where the solid red curve is for $C = -8$ nF, the blue curve is for $C = -6$ nF, and the magenta curve is for $C = -4$ nF. For reference, the long-dashed green curve shows the phase for propagation in vacuum, and the dash-dotted cyan curve shows the phase for unloaded RG-174 coaxial line.

The negative capacitance reduces the magnitude of phase shift relative to the unloaded line for all three negative capacitances. In addition, the magnitude of the phase shift is less than the vacuum case for $C = -8$ nF to just beyond 0.1 MHz, and the phase shift is less than vacuum to nearly 0.09 MHz for $C = -6$ nF. The results closely resemble frequency-scaled versions of earlier results in [2] and [4]. Group delay for S_{21} is plotted in Fig. 4, corresponding to the phase results of Fig. 3. Fast-wave behavior is evidenced by group delay that is less than the vacuum group delay of approx. 300 ns.

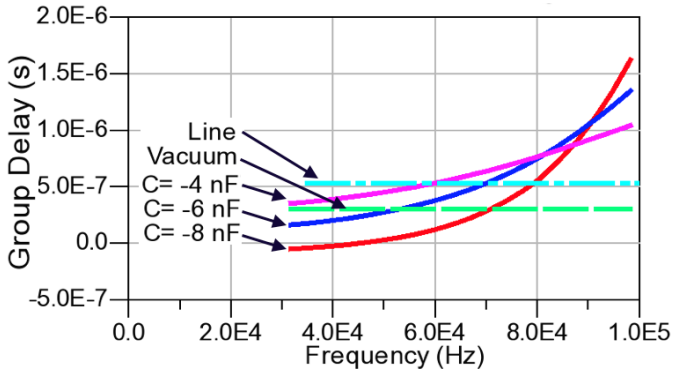

Fig. 4. ADS large-signal S-parameter simulation results, showing group delay corresponding to S_{21} phase given in Fig. 3. Solid red curve is for $C = -8$ nF, blue for $C = -6$ nF, and magenta for $C = -4$ nF. Long-dashed green curve is for propagation in vacuum, and dash-dotted cyan is unloaded RG-174 line.

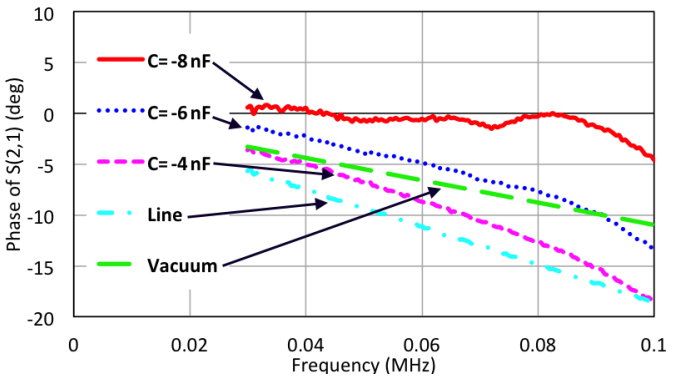

Fig. 5. Measured results for prototype using FRDM-K64F showing phase of S_{21} in degrees for $T = 1\,\mu$s, $R_{dac} = 1000\,\Omega$, $R_1 = 50\,\Omega$ $R_2 = 4700\,\Omega$, latency $\tau = 1\,\mu$s, six 15.25 m long RG-174 line sections, and $H(z)$ in (1). Solid red curve is for $C = -8$ nF, dotted blue for $C = -6$ nF, and dashed magenta for $C = -4$ nF. Long-dashed green curve is for propagation in vacuum, and dash-dotted cyan is unloaded RG-174 line.

IV. Measurements

A prototype of the system of of Fig. 1 was built using three FRDM-K64F microcontroller boards to implement the digital non-Foster circuit of Fig. 2, with the same design parameters as the simulation of Fig. 3. The values of C were varied by changing the signal processing software according to (1). The measured phase of S_{21} is shown in Fig. 5 and corresponds well with the simulation results of Fig. 3, except that the measured phase for $C = -8$ nF appears to have greater bandwidth than in the simulation. The measured $|S_{21}|$ in Fig. 6 shows small gain at upper frequencies, similar to results in [2] and [4].

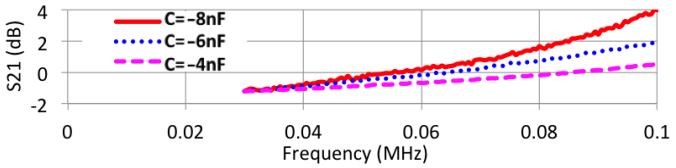

Fig. 6. Measured results for prototype showing $|S_{21}|$ in dB for Fig. 5.

V. Conclusion

Measured and simulation results are in good agreement for a wideband software-adjustable fast-wave line using digital discrete-time non-Foster circuit elements.

Acknowledgement

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References

[1] S. Hrabar, I. Krois, I. Bonic, and A. Kiricenko, "Ultra-broadband simultaneous superluminal phase and group velocities in non-Foster epsilon-near-zero metamaterial," *Applied Physics Letters*, vol. 102, no. 5, pp. 054 108–1–5, 2013.

[2] J. Long, M. Jacob, and D. F. Sievenpiper, "Broadband fast-wave propagation in a non-Foster circuit loaded waveguide," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 789–798, Apr. 2014.

[3] T. P. Weldon, J. M. C. Covington, K. Smith, and R. S. Adams, "Performance of digital discrete-time implementations of non-Foster circuit elements," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2169–2172.

[4] T. P. Weldon and R. S. Adams, "A digital discrete-time non-Foster approach to broadband fast-wave microstrip lines," in *Advanced Electromagnetic Materials in Microwaves and Optics (METAMATERIALS), 2015 9th International Congress on*, Sep. 2015, pp. 322–324.