# Thevenin Forms of Digital Discrete-Time Non-Foster RC and RL Circuits

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***Abstract*—Previous design approaches for digital discrete-time non-Foster circuits have typically employed ideal current-output digital-to-analog converters to establish port currents based on measured voltages. In this paper, the design of digital discrete-time non-Foster circuits is presented for the case of voltage-output digital-to-analog converters with finite source impedance. These finite-impedance converters act as Thevenin sources that can be converted to Norton-equivalent sources for design and analysis. However, it is also straightforward to incorporate the finite source impedance directly into the signal processing, and this is the approach presented. In addition, it is often desirable to add series resistance to improve stability or to mitigate parasitic resistance, so the design of series resistor-capacitor and series resistor-inductor digital discrete-time non-Foster circuits are considered. Finally, unavoidable time-delay latencies associated with conversion time and computation time are also included.**

## I. Introduction

There has been a resurgence of interest in non-Foster circuits such as negative capacitors and negative inductors, in part due to their potential to improve bandwidth and performance in applications as diverse as matching networks, epsilon-near-zero metamaterials, and wideband electrically-small antennas [1]–[3]. Despite considerable progress in analog non-Foster circuit designs for these applications, non-trivial design challenges such as circuit stability remain [4], [5].

More recently, stable digital discrete-time non-Foster circuit designs have been proposed for negative capacitors and negative inductors [6], [7]. The present work extends these prior results by considering the use of a finite-impedance voltage-output DAC (digital-to-analog converter) in place of the prior ideal current-output DAC. This new approach could be adapted to the prior approach using Thévenin-to-Norton transformation. However, the present paper takes a different approach, where the finite source impedance is directly incorporated into the signal processing algorithm, theoretically allowing elimination of the effects of finite source impedance. In addition, digital series RC (resistor-capacitor) and digital series RL (resistor-inductor) circuit implementations are considered, since it is often desirable to add resistance to improve stability or to mitigate parasitic resistance. Finally, the models include latency of conversion time and computation time.

## II. Thévenin Digital RC and RL Circuits

The following sections consider the design of Thévenin-form digital discrete-time non-Foster RC and RL circuits with latency, as shown in Fig. 1. The design follows [6], but using a voltage-output DAC with source impedance $R_{dac}$ in place of an ideal current-output DAC. Continuous-time voltage $v_{in}(t)$ is converted to discrete-time signal $v_{in}[n] = v_{in}(nT)$. Signal processing block $H(z)$ generates $v_{dac}[n] = h[n] * v_{in}[n]$, with z-transform $V_{dac}(z) = H(z)V_{in}(z)$. The DAC output $v_{dac}(t)$ typically includes a ZOH (zero-order hold), and time delay $\tau$ models latency effects due to ADC and DAC conversion time, and computation time. Resistor $R_{dac}$ models the finite source impedance of the DAC, and also sets input current $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$. (Note also that $R_{dac}$ could be replaced by a capacitor, or inductor, or other useful impedance.) The Laplace transform of the DAC output voltage $v_{dac}(t)$ is $V_{dac}(s) = V^{\star}(s)H(z)(1-z^{-1})e^{-s\tau}/s\big|_{z=e^{sT}}$ assuming a zero-order hold in the DAC, and where $V^{\star}(s) = \sum v(nT)e^{-nsT}$, for integer $n$, is the starred transform [8]. The impedance of the non-Foster element of Fig. 1 is then

$$Z(s) \approx \left.\frac{sT\ R_{dac}}{sT - H(z)(1-z^{-1})e^{-s\tau}}\right|_{z=e^{sT}} \tag{1}$$

for $v_{in}(t)$ sampled without aliasing and frequencies below $0.5/T$ Hz.

Next, consider an analog series RC circuit with series resistance $R_{ser}$ (not to be confused with $R_{dac}$ above), where $v(t) = i(t)R_{ser} + \int i(t)dt/C$. Then, taking the derivative yields $dv_{in}(t)/dt = R_{ser}di_{in}(t)/dt + i(t)/C$. Finally, approximating $dv_{in}(t)/dt \approx (v_{in}[n] - v_{in}[n-1])/T$ and $i_{in}[n] \approx [v_{in}[n] - v_{dac}[n]]/R_{dac}$ yields $v_{dac}[n]\,(R_{ser}C + T) = v_{in}[n]\,(R_{ser}C - R_{dac}C + T) + v_{in}[n-1]\,(R_{dac}C - R_{ser}C) +$

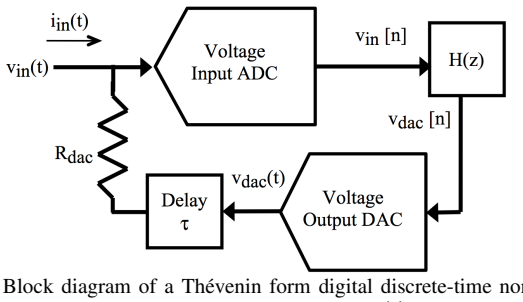


Fig. 1. Block diagram of a Thévenin form digital discrete-time non-Foster circuit element with latency [6]. Input voltage $v_{in}(t)$ is converted by the ADC with clock period $T$ into discrete-time signal $v_{in}[n] = v_{in}(nT)$ and processed by a discrete-time filter with z-transform $H(z)$. DAC output voltage $v_{dac}(t)$ is generated by the DAC from filter output $v_{dac}[n] = h[n] * v_{in}[n]$, and time delay $\tau$ models latency effects. Voltage across $R_{dac}$ sets input current $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$.

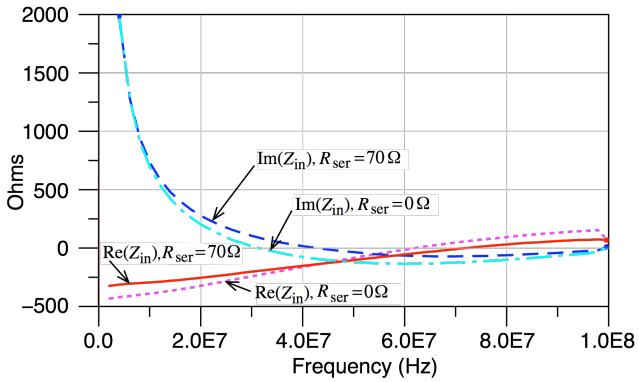


Fig. 2. ADS large-signal S-parameter simulation results for a digital series RC circuit of Fig. 1, where $T = 5$ ns, $C = -25$ pF, $R_{dac} = 1000\,\Omega$, and the latency $\tau = 2.5$ ns. The first simulation is for $R_{ser} = 0\,\Omega$, where the dotted magenta curve is the real part of input impedance $Z(s)$, and cyan dash-dotted curve is the imaginary part. At 10 MHz, the predicted impedance is $-410 + j677$ ohms, and observed impedance is $-406 + j673$ ohms. For $R_{ser} = 70\,\Omega$ the real part of the input impedance is represented by the solid red line and the imaginary part is the blue dashed line. In this case, at 10 MHz the predicted input impedance is $-313 + j722$ ohms from (1) and (2), and the observed impedance is $-310 + j718$ ohms.

$v_{dac}[n-1]R_{ser}C$. Taking the z-transform to solve for $H(z)$ for the RC case results in

$$H_{RC}(z) = \frac{(R_{ser}C - R_{dac}C + T)\,z + (R_{dac}C - R_{ser}C)}{(R_{ser}C + T)\,z - R_{ser}C}. \quad (2)$$

Similarly, consider an analog series RL circuit with series resistance $R_{ser}$, where $v(t) = Ldi(t)/dt + i(t)R_{ser}$. Approximating $di_{in}(t)/dt \approx (i_{in}[n] - i_{in}[n-1])/T$ and with $i_{in}[n] \approx [v_{in}[n] - v_{dac}[n]]/R_{dac}$ yields $v_{dac}[n]\,(1 + R_{ser}T/L) - v_{dac}[n-1] = v_{in}[n]\,(1 + R_{ser}T/L - R_{dac}T/L) - v_{in}[n-1]$. Taking the z-transform to solve for $H(z)$ for the RL case results in

$$H_{RL}(z) = \frac{(L + R_{ser}T - R_{dac}T)\,z - L}{(L + R_{ser}T)\,z - L}. \quad (3)$$

## III. Simulation

A series RC digital discrete-time non-Foster circuit for the system presented in Fig. 1 was simulated in ADS with a capacitance of $C = -25$ pF in series with a resistance $R_{ser}$. The simulation was performed twice, first with $R_{ser} = 0\,\Omega$, and second with $R_{ser} = 70\,\Omega$. For both simulations a clock frequency of 200 MHz was used, corresponding to $T = 5$ ns. The DAC resistance was $R_{dac} = 1000\,\Omega$. Also, a latency of 2.5 ns was added to model the ADC conversion time and computational latency. The results, which display the input impedance $Z(s)$, for both simulations are displayed in Fig. 2. For the first simulation, with $R_{ser} = 0\,\Omega$, the series resistance $\mathrm{Re}\{Z(s)\}$ is represented by the magenta dotted line, and the cyan dash-dotted represents the series reactance $\mathrm{Im}\{Z(s)\}$. The observed impedance at 10 MHz was $-406+j673$ ohms. In the second simulation, with $R_{ser} = 70\,\Omega$, the series resistance is represented by the solid red line and the blue dashed line represents the series reactance. The observed impedance at 10 MHz was $-310 + j718$ ohms; the predicted input impedance was $-313 + j722$ ohms from (1) and (2).

Next, a series RL digital discrete-time non-Foster circuit of Fig. 1 was simulated for an inductance of $L = -2.5$ $\mu$H, $R_{dac} = 1000\,\Omega$, and $T = 5$ ns for two different series resistances, $R_{ser} = 0\,\Omega$ and $R_{ser} = -70\,\Omega$, with $Z(s)$ shown in Fig. 3. For $R_{ser} = 0\,\Omega$, the series resistance $\mathrm{Re}\{Z(s)\}$ is displayed by the magenta dotted line and the series reactance $\mathrm{Im}\{Z(s)\}$ is given by the cyan dash-dotted line, with an observed impedance at 10 MHz of $25 - j165$ ohms. For the second simulation, with $R_{ser} = -70\,\Omega$, the solid red line represents the series resistance, and the blue dashed line represents the series reactance. At 10 MHz the observed impedance was $-38 - j170$ ohms; the predicted input impedance is $-37 - j169$ ohms from (1) and (3).

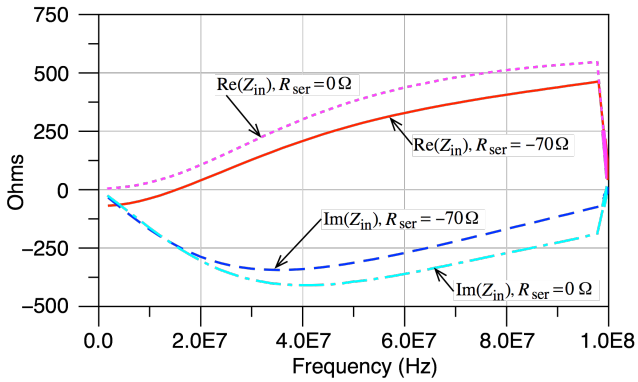


Fig. 3. ADS large-signal S-parameter simulation results for a digital series RL circuit of Fig. 1, where $T = 5$ ns, $L = -2.5$ $\mu$H, $R_{dac} = 1000\,\Omega$, and the latency $\tau = 2.5$ ns. The first simulation is for $R_{ser} = 0\,\Omega$ where the dotted magenta curve is the real part of input impedance $Z(s)$, and cyan dash-dotted curve is the imaginary part. At 10 MHz, the predicted impedance is $24 - j148$ ohms and the observed impedance is $25 - j165$ ohms. For $R_{ser} = -70\,\Omega$ the real part of the input impedance is represented by the solid red line and the imaginary part is the blue dashed line, where at 10 MHz the predicted input impedance is $-37 - j169$ ohms from (1) and (3), and observed impedance is $-38 - j170$ ohms.

## IV. Conclusion

Simulation results for Thévenin forms of digital discrete-time non-Foster RC and RL circuits have been shown to be in good agreement with theoretical predictions.

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