Effects of Latency and Quantization Noise on Digital Discrete-Time Non-Foster Circuits

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***Abstract*—Digital discrete-time implementations of non-Foster circuit elements offer an alternative approach to the design of devices such as negative capacitors and negative inductors. However, practical implementations of high-speed digital non-Foster circuits are affected by latency and noise, where latency can arise from analog-to-digital conversion time and computation time. Thus, the present work explores the impact of latency and quantization noise on digital non-Foster circuits. Simulation results for a digital negative capacitor show useful performance can be obtained, even with latencies as large as one conversion clock cycle. In addition, quantization noise effects in digital non-Foster circuits are considered.**

I. Introduction

Although it has been more than 60 years since Linvill's paper on transistor negative impedance converters, non-Foster circuits such as negative capacitors and negative inductors continue to present design challenges [1]. The unusual electrical characteristics of negative impedances commonly require particular attention to stability issues and noise issues [2], [3]. Nevertheless, there has been a resurgence of interest in applying non-Foster circuits to overcome fundamental limitations in metamaterials and antenna designs [4], [5].

Recently, a digital discrete-time approach to the design of non-Foster circuits has been proposed [6]. This design approach was shown to produce stable digital implementations of non-Foster circuits [7]. However, practical implementation of such digital circuits can be affected by time delays due to ADC (analog-to-digital converter) conversion time, plus the computation time for signal processing. In addition, performance is affected by quantization noise in the ADC and DAC (digital-to-analog converter). The present paper considers the effects of such latencies and quantization noise on the performance of digital discrete-time non-Foster circuit examples.

II. Digital Negative Capacitor with Latency

To illustrate the effect of latency on digital discrete-time non-Foster circuit elements, consider the system of Fig. 1, which is a version of the system in [6], but with latency effects added. The ADC converts continuous-time voltage $v_{in}(t)$ into discrete-time signal $v_{in}[n]$ with sampling period T. Signal processing consists of the convolution $i_{in}[n] = h[n] * v_{in}[n]$, where the z-transform of $h[n]$ is $H(z) = \mathcal{Z}\{h[n]\}$. Next, $i_{in}[n]$ is converted into the continuous-time input current by the DAC, typically with a ZOH (zero-order hold). Finally latency is modeled by adding a time delay τ to the DAC output. Incorporating the effect of the latency time delay into the results in [6], the Laplace transform of the input current is $I_{in}(s) = V^{\star}(s)H(z)(1-z^{-1})e^{-s\tau}/s\big|_{z=e^{sT}}$ where $V^{\star}(s) = \sum v(nT)e^{-nsT}$, for integer n, is the starred transform [8]. The impedance of the non-Foster element of Fig. 1 is then

$$Z(s) = V_{in}(s)/I_{in}(s) \approx sT/[(1-z^{-1})H(z)e^{-s\tau}]\big|_{z=e^{sT}} \ . \quad (1)$$

To illustrate the effect of latency, a negative capacitor design is considered. The negative capacitor in [6] is designed with $H(z)$ denoted as $H_C(z) = C(1-z^{-1})/T$. Substituting this for $H(z)$ in (1) to find the impedance including latency yields:

$$Z_{C\tau}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \frac{sT^2}{[(1-z^{-1})^2 Ce^{-s\tau}]}\bigg|_{z=e^{sT}} , \quad (2)$$

where C is the desired positive or negative capacitance, and $Z_{C\tau}(s)$ is the impedance with a latency of τ seconds.

III. Simulations of Latency Effects

To demonstrate the effect of latency, the digital negative capacitor system in Fig. 1 was simulated using large-signal S-parameters in ADS (as in [6]) for $C = -25$ pF with $T = 5$ ns, and for two different latency values: $\tau = 0$ ns, and $\tau = 5$ ns. Since the clock frequency of the ADC and DAC was 200 MHz, the two latency values represent delays equivalent to zero, and one whole clock cycle. In the simulation results of Fig. 2 and Fig. 3, the solid red line is the real part of the input impedance $Z_{C\tau}(s)$ of Fig. 1, and blue dashed line is the imaginary part.

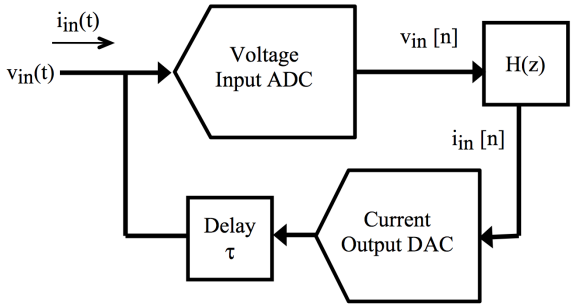

Fig. 1. Block diagram of a digital discrete-time non-Foster circuit element [6]. Input voltage $v_{in}(t)$ is converted by the ADC with clock period T into discrete-time signal $v_{in}[n] = v_{in}(nT)$ and processed by a discrete-time filter with z-transform $H(z)$. Input current $i_{in}(t)$ is generated by the DAC from filter output $i_{in}[n] = h[n] * v_{in}[n]$, and time delay τ models latency effects.

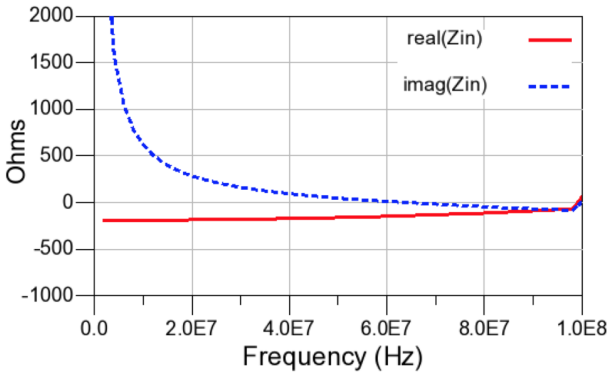

Fig. 2. ADS large-signal S-parameter simulation results for system of Fig. 1 with $T = 5$ ns, $C = -25$ pF, and $\tau = 0$ ns. The solid red curve is the real part of input impedance $Z_{C\tau}(s)$, and dashed blue curve is the imaginary part. The impedance of -25 pF at 10 MHz is $+j637$ ohms, and the observed impedance at 10 MHz is $-194 + j619$ ohms, compared to a theoretical impedance of $-198 + j610$ ohms as predicted in (2).

For this circuit, the predicted reactance of -25 pF at 10 MHz is $+j637$ ohms. Fig. 2 displays input impedance $Z_{C\tau}(s)$, when the latency in the circuit is zero. In this case, the observed impedance was $-194 + j619$ ohms, compared to $-198 + j610$ ohms predicted from (2). Fig. 3 displays $Z_{C\tau}(s)$ when the latency is increased to $\tau = 5$ ns, and the observed impedance becomes $-374 + j528$ ohms, compared to $-377 + j519$ ohms predicted from (2). Comparing Fig. 2 to Fig. 3 at 10 MHz, latency changed parasitic resistance by 90% and reactance by 15%.

IV. Quantization Noise Effects

Quantization noise effects on the digital non-Foster circuit of Fig. 1 may be modeled as shown in the example of Fig. 4. In Fig. 4, the Thévenin source has signal voltage $v_s(t)$, source resistance R_s, and source thermal noise voltage $v_n(t)$ with $\overline{v_n^2} = kT_rBR_s$. Signal $v_q(t)$ is the voltage-input ADC quantization noise voltage with $\overline{v_q^2} = \Delta_v^2/12$, where Δ_v is the ADC voltage step size. Finally, $i_q(t)$ is the quantization noise current of the current-output DAC with $\overline{i_q^2} = \Delta_i^2/12$, where Δ_i is the DAC current step size.

For simplicity, let $h_e(t)$ approximate the effective overall impulse response such that $i_{in}(t) = i_q(t) + [v_{in}(t) + v_q(t)] * h_e(t)$, and substitute $v_{in}(t) = v_s(t) + v_n(t) - i_{in}(t)R_s$. Rearranging in Laplace domain yields

$$I_{in}(s) = \frac{V_s(s)H_e(s)}{1 + H_e(s)R_s} + \frac{I_q(s) + [V_n(s) + V_q(s)]\,H_e(s)}{1 + H_e(s)R_s}, \qquad (3)$$

where the first term represents the signal component of $I_{in}(s)$ dependent on $V_s(s)$, and the second term represents noise.

Next, let $v_s(t)$, $v_n(t)$, $v_q(t)$, and $i_q(t)$ all be uncorrelated with power spectral densities $S_s(\omega)$, $S_n(\omega)$, $S_v(\omega)$, and $S_i(\omega)$, respectively. Then, a noise factor form of a figure of merit for $I_{in}(s)$ can be defined as $F = [S_{in}/N_{in}]/[S_{out}/N_{out}] = \frac{[S_s(\omega)/S_n(\omega)]}{[\{S_s(\omega)|H_e(\omega)|^2\}/\{S_i(\omega)+[S_n(\omega)+S_v(\omega)]|H_e(\omega)|^2\}]}$, yielding:

$$F = 1 + S_v(\omega)/S_n(\omega) + S_i(\omega)/[S_n(\omega)\,|H_e(\omega)|^2] \qquad (4)$$

$$= 1 + \frac{T\Delta_v^2/12}{kT_rR_s} + \frac{T\Delta_i^2/12}{kT_rR_s\,|H_e(\omega)|^2}, \qquad (5)$$

where it is noted that this F only applies to the example of Fig. 4, and $H_e(\omega)$ results in potentially useful noise shaping.

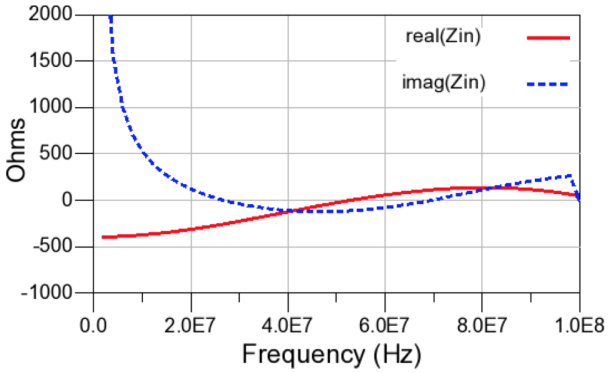

Fig. 3. ADS large-signal S-parameter simulation results for system of Fig. 1 with $T = 5$ ns, $C = -25$ pF, and $\tau = 5$ ns. The solid red curve is the real part of input impedance $Z_{C\tau}(s)$, and dashed blue curve is the imaginary part. The impedance of -25 pF at 10 MHz is $+j637$ ohms, and the observed impedance at 10 MHz is $-374 + j528$ ohms, compared to a theoretical impedance of $-377 + j519$ ohms as predicted in (2).

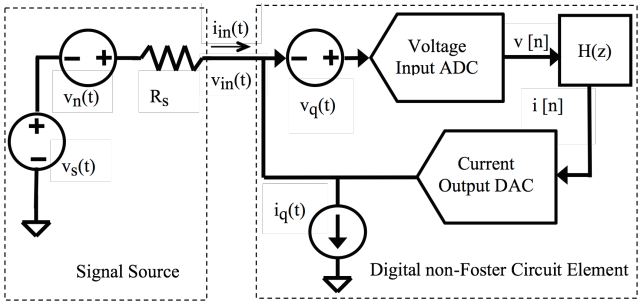

Fig. 4. Noise model with noisy Thévenin signal source with source resistance R_s, where $v_s(t)$ is the signal voltage, $v_n(t)$ is the thermal noise voltage with $\overline{v_n^2} = kT_rBR_s$, $v_q(t)$ is voltage-input ADC quantization noise voltage with $\overline{v_q^2} = \Delta_v^2/12$ where Δ_v is voltage step size, and $i_q(t)$ is current-output DAC quantization noise current with $\overline{i_q^2} = \Delta_i^2/12$ where Δ_i is current step size.

V. Conclusion

Analysis and simulation of effects of latency and quantization noise on digital non-Foster circuits have been presented.

References

[1] J. Linvill, "Transistor negative-impedance converters," *Proc. of the IRE*, vol. 41, no. 6, pp. 725–729, Jun. 1953.

[2] S. D. Stearns, "Stable band-pass non-Foster circuits," in *Antennas and Propagation USNC/URSI National Radio Science Meeting, 2015 IEEE International Symposium on*, July 2015, pp. 1386–1387.

[3] M. M. Jacob, J. Long, and D. F. Sievenpiper, "Noise in non-Foster antenna matching circuits," in *Antennas and Propagation Society International Symposium (APSURSI), 2013 IEEE*, Jul. 2013, pp. 2205–2206.

[4] S. Hrabar, I. Krois, I. Bonic, and A. Kiricenko, "Ultra-broadband simultaneous superluminal phase and group velocities in non-Foster epsilon-near-zero metamaterial," *Applied Physics Letters*, vol. 102, no. 5, pp. 054 108–1–5, 2013.

[5] N. Zhu and R. W. Ziolkowski, "Active metamaterial-inspired broadbandwidth, efficient, electrically small antennas," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1582–1585, 2011.

[6] T. P. Weldon, J. M. C. Covington, K. Smith, and R. S. Adams, "Performance of digital discrete-time implementations of non-Foster circuit elements," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2169–2172.

[7] T. P. Weldon, J. M. C. Covington, K. Smith, and R. S. Adams, "Stability conditions for a digital discrete-time non-Foster circuit element," in *2015 IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Jul. 2015.

[8] C. Phillips and H. Nagle, *Digital Control System Analysis and Design*. Prentice-Hall, 1990.