Effects of Latency and Quantization Noise on Digital Discrete-Time Non-Foster Circuits

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Abstract—Digital discrete-time implementations of non-Foster circuit elements offer an alternative approach to the design of devices such as negative capacitors and negative inductors. However, practical implementations of high-speed digital non-Foster circuits are affected by latency and noise, where latency can arise from analog-to-digital conversion time and computation time. Thus, the present work explores the impact of latency and quantization noise on the performance of digital discrete-time non-Foster circuits. Simulation results for a digital negative capacitor show useful performance can be obtained, even with latencies as large as one conversion clock cycle. In addition, quantization noise effects in digital non-Foster circuits are considered.

I. INTRODUCTION

Although it has been more than 60 years since Linvill’s paper on transistor negative impedance converters, non-Foster circuits such as negative capacitors and negative inductors continue to present design challenges [1]. The unusual electrical characteristics of negative impedances commonly require particular attention to stability issues and noise issues [2], [3]. Nevertheless, there has been a resurgence of interest in applying non-Foster circuits to overcome fundamental limitations in metamaterials and antenna designs [4], [5].

Recently, a digital discrete-time approach to the design of non-Foster circuits has been proposed [6]. This design approach was shown to produce stable digital implementations of non-Foster circuits [7]. However, practical implementation of such digital circuits can be affected by time delays due to ADC (analog-to-digital converter) conversion time, plus the computation time for signal processing. In addition, performance is affected by quantization noise in the ADC and DAC (digital-to-analog converter). The present paper considers the effects of such latencies and quantization noise on the performance of digital discrete-time non-Foster circuit examples.

II. DIGITAL NEGATIVE CAPACITOR WITH LATENCY

To illustrate the effect of latency on digital discrete-time non-Foster circuit elements, consider the system of Fig. 1, which is a version of the system in [6], but with latency effects added. The ADC converts continuous-time voltage \(v_{in}(t)\) into discrete-time signal \(v_{in}[n]\) with sampling period \(T\). Signal processing consists of the convolution \(i_{in}[n] = h[n] * v_{in}[n]\), where the z-transform of \(h[n]\) is \(H(z) = \mathcal{Z}\{h[n]\}\). Next, \(i_{in}[n]\) is converted into the continuous-time input current by the DAC, typically with a ZOH (zero-order hold). Finally latency is modeled by adding a time delay \(\tau\) to the DAC output. Incorporating the effect of the latency time delay into the results in [6], the Laplace transform of the input current is \(I_{in}(s) = V^*\{s\}H(z)(1 - z^{-1})e^{-s\tau}/s\) where \(V^*\{s\} = \sum v(nT)e^{-nsT}\), for integer \(n\), is the starred transform [8]. The impedance of the non-Foster element of Fig. 1 is then

\[
Z(s) = V_{in}(s)/I_{in}(s) \approx sT/[1 - z^{-1}]H(z)e^{-\tau s}\]  

(1)

To illustrate the effect of latency, a negative capacitor design is considered. The negative capacitor in [6] is designed with \(H(z)\) denoted as \(H_C(z) = C(1 - z^{-1})/T\). Substituting this for \(H(z)\) in (1) to find the impedance including latency yields:

\[
Z_C(s) = V_{in}(s)/I_{in}(s) \approx sT^2/[(1 - z^{-1})^2Ce^{-\tau s}]_{z=e^{\tau s}}\]  

(2)

where \(C\) is the desired positive or negative capacitance, and \(Z_C(s)\) is the impedance with a latency of \(\tau\) seconds.

III. SIMULATIONS OF LATENCY EFFECTS

To demonstrate the effect of latency, the digital negative capacitor system in Fig. 1 was simulated using large-signal S-parameters in ADS (as in [6]) for \(C = -25\) pF with \(T = 5\) ns, and for two different latency values; \(\tau = 0\) ns, and \(\tau = 5\) ns. Since the clock frequency of the ADC and DAC was 200 MHz, the two latency values represent delays equivalent to zero, and one whole clock cycle. In the simulation results of Fig. 2 and Fig. 3, the solid red line is the real part of the input impedance \(Z_C(s)\) of Fig. 1, and blue dashed line is the imaginary part.

Fig. 1. Block diagram of a digital discrete-time non-Foster circuit element [6]. Input voltage \(v_{in}(t)\) is converted by the ADC with clock period \(T\) into discrete-time signal \(v_{in}[n] = v_{in}(nT)\) and processed by a discrete-time filter with z-transform \(H(z)\). Input current \(i_{in}(t)\) is generated by the DAC from filter output \(i_{in}[n] = h[n] * v_{in}[n]\), and time delay \(\tau\) models latency effects.
For this circuit, the predicted reactance of \(-25\) pF at 10 MHz is \(+j637\) ohms, compared to a theoretical reactance of \(-194 + j619\) ohms, compared to a theoretical reactance of \(-198 + j610\) ohms as predicted in (2).

IV. QUANTIZATION NOISE EFFECTS

Quantization noise effects on the digital non-Foster circuit of Fig. 1 may be modeled as shown in the example of Fig. 4. In Fig. 4, the Thévenin source has signal voltage \(v_s(t)\), source resistance \(R_s\), and source thermal noise voltage \(v_{n}(t)\) with \(v_n^2 = kTBR_s\). Signal \(v_s(t)\) is the voltage-input ADC quantization noise voltage with \(v_q^2 = \Delta_q^2/12\), where \(\Delta_q\) is the ADC voltage step size. Initially, \(i_q(t)\) is the quantization noise current of the current-output DAC with \(\Delta_i^2 = \Delta_q^2/12\), where \(\Delta_i\) is the DAC current step size.

For simplicity, let \(h_e(t)\) approximate the effective overall impulse response such that \(i_{in}(t) = i_q(t) + [v_{in}(t) + v_q(t)]\) *.