Reduced Current Class AB Radio Receiver Stages Using Novel Superlinear Transistors with Parallel NMOS and PMOS Transistors at One GHz

Don T. Lieu
University of North Carolina at Charlotte
Charlotte, NC, 28223, USA
dtlieu@uncc.edu

Thomas P. Weldon
University of North Carolina at Charlotte
Charlotte, NC, 28223, USA
tpweldon@uncc.edu

Abstract

Class AB amplifier stages are commonly used to conserve power in radio transmitters. In this paper, a Class AB amplifier stage is investigated for use in radio receivers to reduce power consumption. In this, a novel superlinear three-terminal transistor consisting of an NMOS transistor in parallel with a PMOS transistor is used to improve Class AB linearity to a level approaching Class A performance. Optimum transistor bias conditions for the linearized Class AB receiver stage are also presented. Measured and simulated results at 1 GHz show supply current reduction of approximately 40 percent and 4 dB improvement in third order intercept point using linearization. Finally, simulations of an improved Class AB design show third order output intercept better than a corresponding Class A stage and show more than 50 percent reduction in power consumption.

1. Introduction

As the power efficiency of radio transmitters improves, the power consumption of receiver stages becomes more significant in battery-powered radios [1]. As a result, improvements in receiver power consumption are becoming an increasingly important in improving battery life. Unfortunately, such efforts to reduce receiver power consumption are frequently constrained by conflicting system requirements for large dynamic range and high third-order intercept point.

To address these issues, a Class AB receiver design is proposed. Although this Class AB approach appears straightforward, the reduced bias of Class AB stages is typically accompanied by reduced linearity at low and moderate signal levels. Such reduced linearity can cause undesired intermodulation and signal blocking at low and moderate signal levels, below Class AB self-biasing signal levels. To offset such reduced linearity at low signal levels, a linearization method is also proposed.

In prior work, Xiong and Larson proposed a Class AB LNA using an adaptive bias circuit [2], but did not linearize the circuit at low or moderate signal levels. The proposed approach in the present paper addresses this limitation, since it incorporates a linearization method. In other work, a variety of linearization methods have been proposed for use in power amplifiers [3]-[10]. Unfortunately, most of these power amplifier linearization methods require prior knowledge of the signal or an undistorted reference signal which would not be available in a receiver application. Finally, Wang et al., present a power amplifier linearization method that uses PMOS gate capacitance to linearize an NMOS device [3]. However, the outputs of the two transistors are not coupled in Wang et al., and their target application is again power amplifiers instead of receivers.

Therefore, a novel linearized Class AB receiver stage is proposed for reduced power consumption in radio receivers. Following earlier results [11]-[12], a Class AB amplifier stage is linearized using a simple approach where third order distortion is canceled using a PMOS transistor in parallel with an NMOS transistor. In this, the PMOS device is designed such that its third order distortion cancels the third order distortion of the NMOS device. Furthermore, the basic linearization technique can be applied to linearize other devices (BJT, JFET, etc.), does not require external passive components, and is readily implemented in CMOS integrated circuits.

In addition, results are presented that show linearization performance as a function of bias conditions and geometry for the PMOS and NMOS transistors. Device geometries may be optimized for different levels of linearization performance, and device bias can be used to implement adaptive or static Class AB performance. The free design parameters of device geometry and device bias can be used to optimize designs for linearity, dynamic range, and power consumption in specific applications.

In the following sections, the design of the Class A and Class AB stages are first outlined. Next, the basic linearization approach is described. Then, measured results at 1.0 GHz are presented for Class A, Class AB, and linearized Class AB designs. It is shown that the linearized Class AB design has small-signal linearity that equals or exceeds that of the Class A design, but with only 60% of the Class A power consumption.

2. Approach

For the purpose of evaluating the new method, an NMOS Class A amplifier reference design will first be considered. Then, a non-linearized Class AB stage is designed with bias of approximately 50% of the Class A reference design. Finally, a linearized Class AB stage is designed with bias of approximately 60% of the Class A reference design, using a PMOS transistor in parallel with NMOS transistor for linearization. The power consumption and linearity of the Class AB design and linearized Class AB design are then compared to the Class A reference design. The overall result is that the linearized Class AB has reduced power consumption while retaining linearity that approaches or exceeds the linearity of the Class A design.

Before proceeding, the basic linearization approach shown in Fig. 1(a) is described. In this, two amplifiers with different gains and intercept points are combined in parallel. Following previous results in [11] – [12], the overall circuit of Fig. 1(a) is linearized when:

$$3(G_1 - G_2) = 2(OIP3_1 - OIP3_2) \ , \qquad (1)$$

where G1 ≠ G2, G1 and G2 are the gains in dB of U1 and U2, and OIP31 and OIP32 are the output third order intercept points of U1 and U2.

In the present case of CMOS amplifiers, Fig. 2(b) shows the proposed linearized Class AB design consisting of an NMOS transistor in parallel with a PMOS transistor. The NMOS transistor would correspond to amplifier U1, and the PMOS transistor would correspond to amplifier U2 of Fig. 1(a). The inductor shown is a simple RF choke DC feed. Since the outputs of the PMOS transistor and NMOS transistor are out of phase, the subtraction if Fig 1(a) is also implemented at the output in Fig. 1(b). Although the analysis of Fig. 2(b) is somewhat more complex, having the amplified output of the NMOS transistor increase the V_{gs} of the PMOS transistor, the basic notion of Fig. 1(a) underlies the design.

The Class A amplifier reference design is shown in Fig. 2, consisting of a simple NMOS common-source amplifier. The Class A design of Fig. 2 essentially corresponds to the design of Fig. 1(b) without a PMOS device. In Fig. 2, a DC bias voltage is applied along with the input signal at the input port, Pin. The drain is biased through an RF choke, with final output taken at port Pout typically through AC coupling.

The non-linearized Class AB amplifier design is also given by Fig. 2, except that gate bias is reduced to result in approximately half the current of the original Class A design.

Finally, the linearized Class AB amplifier design is shown in Figure 1(b). As outlined in the introduction, the Class AB has poor linearity relative to the Class A design

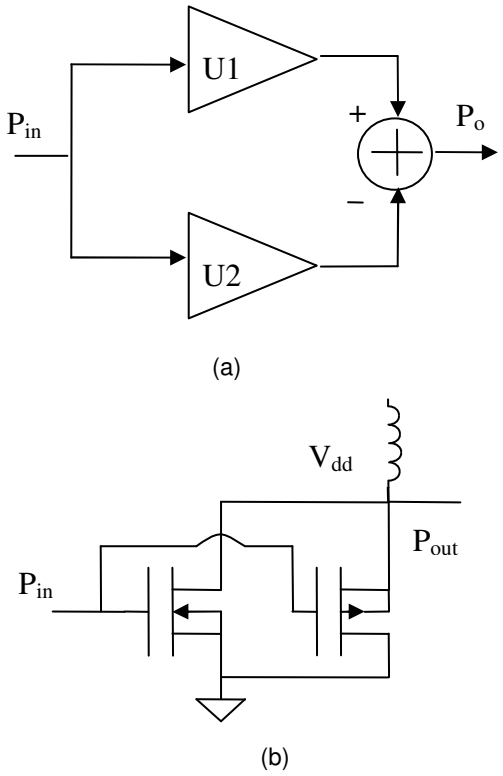

Figure 1. Top figure (a) illustrating linearization approach consisting of main amplifier U1, compensating amplifier U2, with output of U2 subtracted from output of U1. Bottom figure (b) showing proposed linearized Class AB circuit consisting of an NMOS transistor in parallel with a PMOS transistor, corresponding to U1 and U2 respectively.

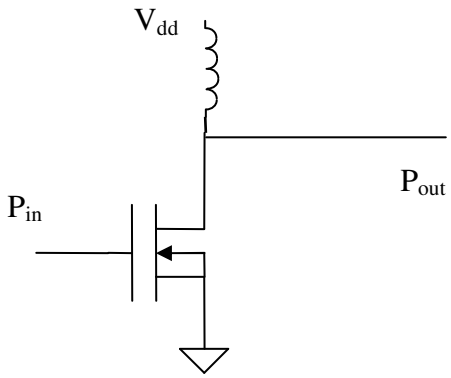

Figure 2. Class A amplifier reference design using an NMOS transistor; Class AB circuit is identical, but with reduced gate bias and reduced drain current.

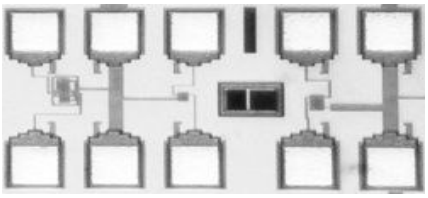

Figure 3. Photograph of chip showing linearized Class AB PMOS+NMOS amplifier on left, and Class A and AB device on right.

because of the reduced bias levels. To improve Class AB linearity, the approach of Fig. 1 is employed as described in [11]-[12]. In this, the third order nonlinearities at the output of amplifier U1 are cancelled by subtracting the third order nonlinearities at the output of amplifier U2. For good linearization without losing gain, the gain of the second amplifier should be much smaller than the gain of the first amplifier [12].

The geometry of the Class AB NMOS transistor in Fig. 1(b) is the same as that of Class A amplifier in Fig. 2. The geometry and bias point of the PMOS device is selected to give optimal linearity. In addition, the circuit of Fig. 1(a) allows flexibility in using the bias point to tune for maximum linearity. In this, variation in V_{dd} primarily affects the bias of the PMOS device, since V_{dd} also changes V_{gs} of the PMOS device. For fixed input gate bias, V_{dd} can then be adjusted to optimize linearity. Although the linearization method of Fig. 1 is chosen for simple implementation in a CMOS processes and to illustrate the overall approach, alternative methods could be used [12].

3. Results

The Class A, non-linearized Class AB, and linearized Class AB amplifiers were fabricated in TSMC 0.18 um technology, shown in Fig. 3. In all three amplifier designs, the size of the NMOS transistor was 121×0.18 µm. The size of the PMOS transistor in the linearized Class AB design was 30×0.18 µm.

Table I shows the bias and OIP3 (third order output intercept point) of the three designs. All three designs had a an output bias of V_{dd} = 1.9 V. The Class A design was biased with V_{gs} = 1.0 V, resulting in a drain current of 21.2 mA. Similarly, the non-linearized Class AB was biased with V_{gs} = 0.78 V at 9.6 mA. The linearized Class AB design was biased with NMOS gate voltage V_{gs} = 0.78 V at 12.1 mA total for both the PMOS and NMOS devices. The 18.9 dBm OIP3 of the linearized Class AB is significantly better than the 14.9 dBm non-linearized Class AB, although not quite meeting the 25 dBm performance of the Class A design. The linearization resulted in 4 dB, or 150 percent, increase in third-order intercept point with only 26 percent increase in current.

Table I. Measured Results.

Design	V_{GS} (V)	I_D (mA)	OIP3 (dBm)
Class A	1	21.2	25.1
Class AB	0.78	9.6	14.9
Linearized Class AB	0.78	12.1	18.9

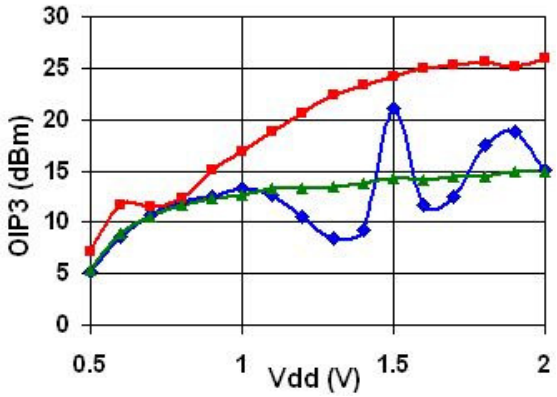

Figure 4. Measured OIP3 vs Vdd at 1GHz. The red square, green triangle, and blue diamond represent Class A, Class AB, and linearized Class AB respectively. Vertical axis is OIP3 in dBm.

Fig. 4 shows measured OIP3 as a function of V_{dd} at 1 GHz for all three designs, using the aforementioned input gate bias voltages, Vgs. From Fig. 4, the optimum linearized Class AB bias points are at V_{dd} = 1.9 V or at V_{dd} = 1.5 V. Fig. 5 shows simulation results corresponding to Fig. 4. Figs. 4 and 5 are quite similar, except for the magnitude of the linearized Class AB peak in OIP3 near V_{gs} = 1.4 V. Nevertheless, the measured and simulated results correspond quite well.

Fig. 6 shows measured OIP3 as a function of input power level P_{in} at 1 GHz for all three designs, using the Table I input gate bias voltages, V_{gs}. In this plot, the linearized Class AB design has better OIP3 than the non-linearized Class AB design at low and intermediate signal levels. Fig. 7 shows simulation results corresponding to the measured results of Fig. 6.

Based on results from the foregoing design, simulations were performed on an improved design,. In this new design, the NMOS is resized to 120×0.18 µm and the PMOS device 11×0.18 µm. With the new design, the simulated linearized Class AB OIP3 exceeds the Class A OIP3 as shown in Fig. 8. In this modified design, the bias voltages are V_{gs} = 1.1 V at 25.9 mA for Class A, V_{gs} = 0.8

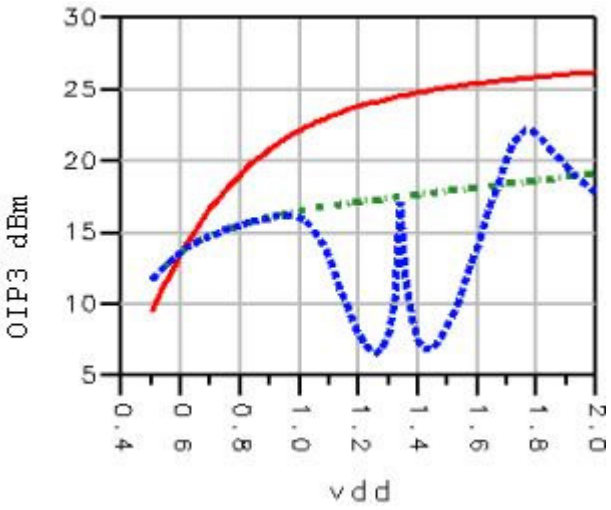

Figure 5. Simulation results: OIP3 vs Vdd at 1GHz. The solid red, dash-dotted green, and dashed blue lines are the Class A, Class AB, and linearized Class AB.

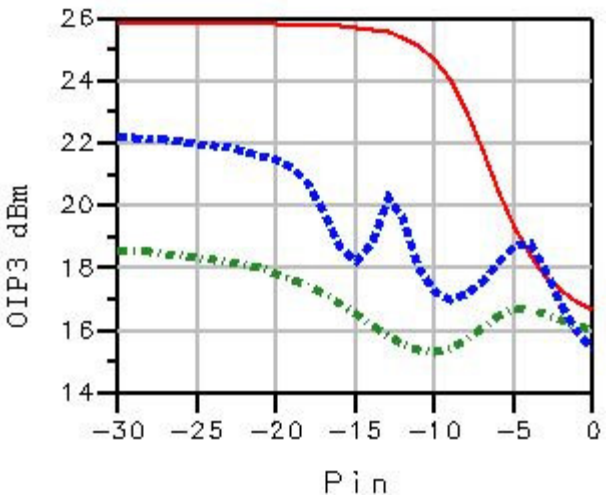

Figure 7. Simulation results: OIP3 vs Pin at 1GHz. The solid red, dash-dotted green, and dashed blue lines are the Class A, Class AB, and linearized Class AB.

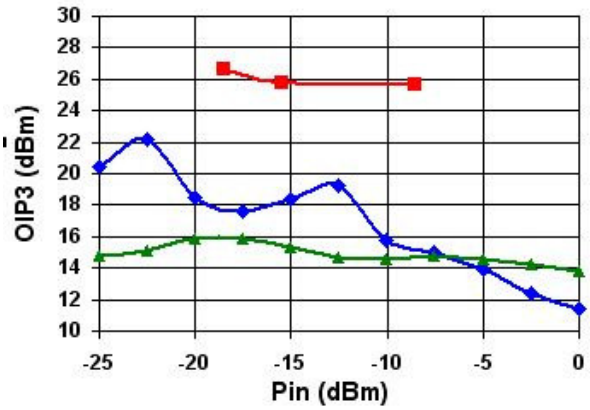

Figure 6. Measured OIP3 vs Pin at 1GHz. The red square, green triangle, and blue diamond represent Class A, Class AB, and linearized Class AB respectively. Vertical axis is OIP3 in dBm.

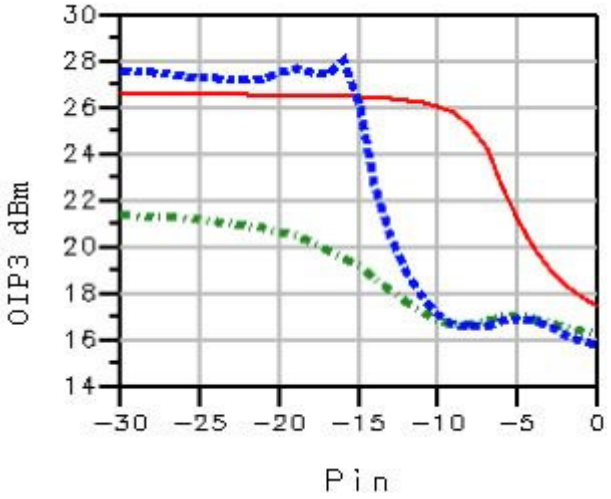

Figure 8. Simulation results: OIP3 vs Pin at 1GHz for optimum geometry NMOS 120 x 0.18 um and PMOS 11 x 0.18 um. The solid red, dash-dotted green, and dashed blue lines are the Class A, Class AB, and linearized Class AB.

V at 10.9 mA for Class AB, V_{gs} = 0.8 V at 11.7 mA for linearized Class A (a 55% current reduction). V_{dd} was 1.86 V for all three designs.

4. Conclusion

A linearized Class AB amplifier for receiver application was demonstrated with reduced power consumption relative to a conventional Class A design. Measured results showed that the proposed linearization method improved third-order intercept point by 4 dB, with current consumption reduction of more than 40 percent. Finally, simulations of an improved design show potential for a linearized Class AB design with third order output intercept better than the Class A design and with over 50 percent reduction in power consumption.

5. Acknowledgements

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6. References

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