Measurement of a Digital Non-Foster Negative RLC Circuit and Digital Positive RLC Circuit

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***Abstract*—Measurements and theory are presented for digital discrete-time implementations of series non-Foster negative RLC (resistor-inductor-capacitor) circuits and series positive RLC circuits. This new digital RLC design approach builds upon recent digital implementations of other non-Foster circuits such as negative RC (resistor-capacitor) and negative RL (resistor-inductor) circuits. Such digital implementations of non-Foster circuits have shown promise in addressing common design challenges, such as stability, that may be more difficult to control in analog non-Foster circuits. Furthermore, a digital approach offers inherent potential advantages in applications such as software-tunable or adaptive digital implementations of negative RLC or positive RLC circuits. To confirm the proposed approach and underlying theory, simulation results and prototype measurements are provided that demonstrate the efficacy of digital implementations of both positive RLC and negative RLC circuits.**

I. Introduction

Non-Foster circuits, such as negative capacitors and negative inductors, have the potential to improve the performance of a wide range of existing technologies such as impedance matching networks [1], electrically small antennas [2], [3], and software defined radios [4], [5] as well as enabling a number of unusual emerging technologies such as magnetic conductors [6], microwave metamaterials [7], [8], and acoustic invisibility [9], [10]. Although analog non-Foster circuits were first realized over 60 years ago [11], difficult design challenges such as circuit stability remain. Digital discrete-time implementations of non-Foster circuits, recently pioneered in [12], have the potential to offer solutions to previous design challenges by leveraging advantages of digital technologies. Furthermore, digital implementations of non-Foster circuits are likely to be advantageous in the design of adaptive and software-tunable systems [13].

The current work extends the digital discrete-time non-Foster RC circuit of [14] to a Thévenin-form digital non-Foster series RLC (resistor-inductor-capacitor) circuit. Prior non-Foster RLC circuits have been limited to analog implementations [15]–[17]. Strictly, a Foster circuit is comprised only of lossless positive inductors and capacitors [18]. Hence, circuits containing negative capacitors and/or negative inductors are often loosely referred to as non-Foster circuits. In the following, "negative RLC" refers to circuits having negative capacitance and negative inductance. The proposed approach implements positive or negative RLC digitally, using an ADC (analog-to-digital converter), digital signal processing, and DAC (digital-to-analog converter). Also, stability conditions are are determined for the *digital positive RLC* and *digital negative RLC* cases.

In the following section, digital discrete-time theory for a digital RLC circuit is presented. Section III provides root locus stability analysis to determine stable regions of operation. Simulation and measurement results, which compare favorably with theoretical values, are presented and discussed in sections IV and V, respectively.

II. Digital Discrete-Time RLC Theory

The desired (positive or negative) analog series RLC behavior is illustrated in Fig. 1(a), and the block diagram of the proposed digital RLC implementation is shown in Fig. 1(b). *The objective is to design signal prcessing $H(z)$ such that the impedance looking into the right-hand dashed box of Fig. 1(b) approximates the desired analog series RLC impedance of Fig. 1(a).* The approach of Fig. 1(b) builds upon digital non-Foster RC and RL results in [14], but with new signal

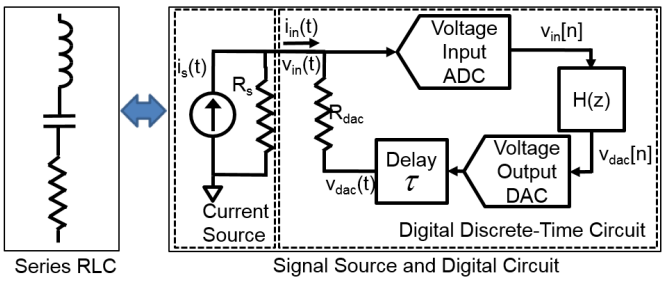

Fig. 1. (a) On the left side of the image is a series analog RLC circuit which is implemented in discrete-time through signal processing block $H(z)$. (b) The block diagram of a Thévenin form digital discrete-time circuit is shown on right side of image [12]. Analog input voltage $v_{in}(t)$ is converted into discrete-time signal $v_{in}[n] = v_{in}(nT)$ by the ADC with clock period T. The signal is then processed by discrete-time filter $H(z)$ resulting in $v_{dac}[n] = h[n] * v_{in}[n]$, which is then converted into analog $v_{dac}(t)$ by the DAC. The DAC output resistance is modeled as R_{dac} and time delays are modeled as latency τ. The circuit is driven by an external Norton current source $i_s(t)$ with source resistance R_s [19].

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processing $H(z)$ designed for for implementation of a digital negative RLC circuit and a digital positive RLC circuit.

Consider the digital discrete-time circuit in the right-hand dashed box of Fig. 1(b). Analog input voltage $v_{in}(t)$ is converted by the ADC with clock period T into discrete-time signal $v_{in}[n] = v_{in}(nT)$. Next, the signal passes through digital signal processing block $H(z)$, generating convolution output $v_{dac}[n] = h[n] * v_{in}[n]$, where $H(z)$ is the z-transform of $h[n]$. Lastly, $v_{dac}[n]$ is converted into analog signal $v_{dac}(t)$ by the DAC. Latency effects are included as time delay τ, and can arise from ADC and DAC conversion times, and from computation time. The input current is then $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$, where resistor R_{dac} is the Thévenin source impedance of the DAC. The Laplace transform of $v_{dac}(t)$, under the assumption the DAC has a ZOH (zero order hold), is $V_{dac}(s) = V^{\star}(s)H(z)\left(1 - z^{-1}\right)e^{-s\tau}/s\big|_{z=e^{sT}}$, where $V^{\star}(s) = \sum v(nT)e^{-nsT}$ is the starred transform [20]. The input impedance of the digital discrete-time circuit in the right-hand dashed box of Fig. 1(b) is then [14]

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \left.\frac{sTR_{dac}}{sT - H(z)\left(1 - z^{-1}\right)e^{-s\tau}}\right|_{z=e^{sT}}, \quad (1)$$

for signals without aliasing and for frequencies below $0.5/T$ Hz.

Next, consider an analog series RLC circuit as shown on the left in Fig. 1, where $v_{in}(t) = i_{in}(t)R_{ser} + Ldi_{in}(t)/dt + \int i_{in}(t)dt/C$. Taking the derivative yields $dv_{in}(t)/dt = R_{ser}di_{in}(t)/dt + Ld^2i_{in}(t)/dt^2 + i_{in}(t)/C$. Approximating $dv_{in}(t)/dt = (v_{in}[n] - v_{in}[n-1])/T$ and $di_{in}(t)/dt = (i_{in}[n] - i_{in}[n-1])/T$ results in $(v_{in}[n] - v_{in}[n-1])/T = R_{ser}(i_{in}[n] - i_{in}[n-1])/T + L(i_{in}[n] - 2i_{in}[n-1] + i_{in}[n-2])/T^2 + i_{in}[n]/C$. Then, substituting $i_{in}[n] = (v_{in}[n] - v_{dac}[n])/R_{dac}$ results in

$$\begin{aligned}\frac{v_{in}[n] - v_{in}[n-1]}{T} &= \\ &\frac{R_{ser}}{TR_{dac}}(v_{in}[n] - v_{in}[n-1] - v_{dac}[n] + v_{dac}[n-1]) \\ &+ \frac{L}{R_{dac}T^2}\Big(v_{in}[n] - 2v_{in}[n-1] + v_{in}[n-2] \\ &\qquad - v_{dac}[n] + 2v_{dac}[n-1] - v_{dac}[n-2]\Big) \\ &+ \frac{1}{CR_{dac}}\left(v_{in}[n] - v_{dac}[n]\right).\end{aligned} \quad (2)$$

After rearranging and taking the z-transform, the transfer function for the series RLC circuit becomes

$$\begin{aligned}H_{RLC}(z) = V_{dac}(z)/V_{in}(z) = \\ \frac{(T^2 + LC - CR_{dac}T + CR_{ser}T)z^2}{(T^2 + CR_{ser}T + LC)z^2 + (-2LC - CR_{ser}T)z + LC} \\ + \frac{(CR_{dac}T - 2LC - CR_{ser}T)z \;+\; LC}{(T^2 + CR_{ser}T + LC)z^2 + (-2LC - CR_{ser}T)z + LC}.\end{aligned} \quad (3)$$

Note that the foregoing relations apply for implementations of digital negative RLC circuits (with L and C negative) as well as digital positive RLC circuits (with L and C positive).

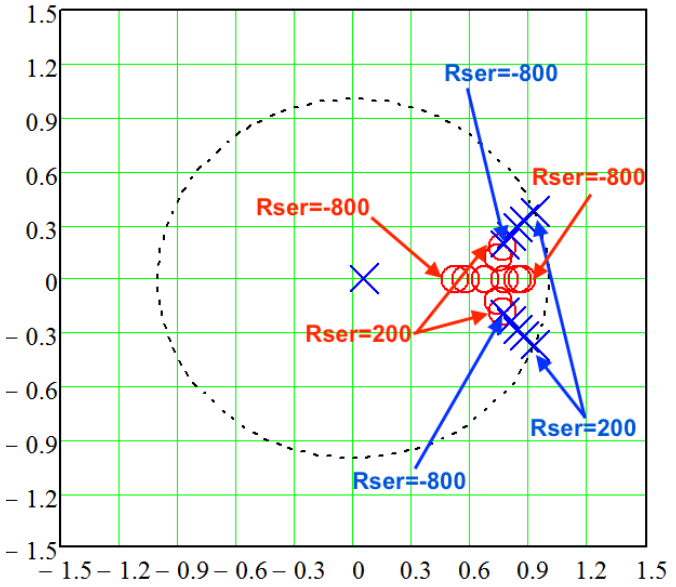

Fig. 2. Root locus stability analysis performed on (4) for a digital non-Foster negative RLC example, varying R_{ser} from -800 ohms to 200 ohms, with stability for $R_{ser} < 200$ ohms, and instability for $R_{ser} > 200$ ohms. Other system parameters were $T = 1.22$ μs, $C = -5$ nF, $L = -2$ mH, $R_{dac} = 1000$ ohms, and $\tau = 1.22$ μs. Poles are represented by "X" and zeros by "O". Rs=50.

III. Stability Analysis

For the purpose of stability analysis, the discrete-time closed-loop pulse transfer function of the current source and digital discrete-time circuit, of Fig. 1(b), must be examined. Consider the closed-loop transfer function $G(s) = I_{in}(s)/I_s(s)$, where $I_{in}(s)$ is the current seen at the input to the digital circuit inside the dashed box on the right of Fig. 1(b), and $I_s(s)$ is the source current in the dashed box on the left of Fig. 1(b). The corresponding discrete-time closed-loop pulse transfer function $G(z)$ is then [20]

$$G(z) = \frac{I_{in}(z)}{I_s(z)} = \frac{R_e z^{-\lambda}H(z)/R_{dac}}{1 + R_e z^{-\lambda}H(z)/R_{dac}}, \quad (4)$$

where $R_e = R_s R_{dac}/(R_s + R_{dac})$ is the parallel combination of the DAC output resistance and the signal source impedance, λ is the latency in clock cycles with $\tau = \lambda T$, and $V_{in}(z)H(z)z^{-\lambda}/R_{dac}$ would be the Norton-equivalent current of the Thévenin source comprised of the voltage-output DAC in series with R_{dac} on the right of Fig. 1(b). The system is stable as long as the poles of $G(z)$ lie within the unit circle [20].

A root locus analysis is used (4) to determine the stability of the system in Fig. 1(b) when $H(z) = H_{RLC}(z)$ for both a negative RLC example and a positive RLC example, as the series resistance parameter R_{ser} is varied. The root locus is shown in Fig. 2 for a negative non-Foster RLC example, and in Fig. 3 for a positive RLC example.

For the negative RLC case of Fig. 2, R_{ser} is varied from $R_{ser} = -800$ ohms to $R_{ser} = 200$ ohms in steps of 250 ohms. Other system parameters were $T = 1.22$ μs, $C = -5$ nF, $L = -2$ mH, $R_{dac} = 1000$ ohms, $\lambda = 1$, and $\tau = 1.22$ μs. In Fig. 2, the edge of stability occurs at $R_{ser} \approx 200$ ohms

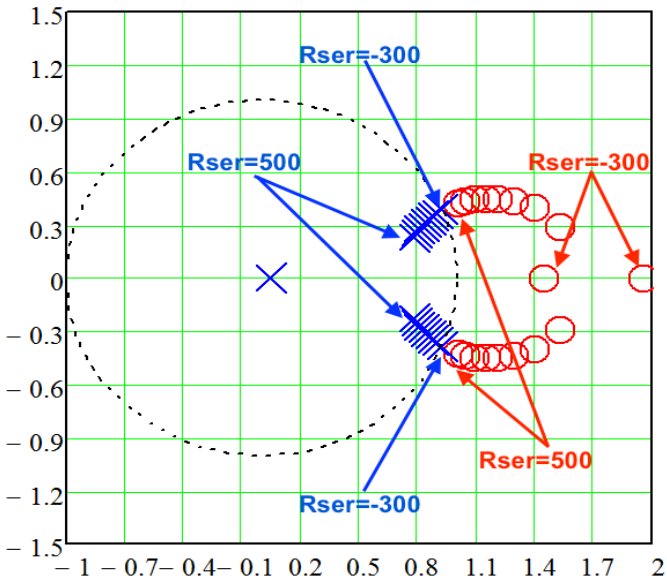

Fig. 3. Root locus stability analysis performed on (4) for a digital positive RLC example, varying R_{ser} from -300 to 500 ohms, with stability for $R_{ser} > -300$ ohms, and instability for $R_{ser} < -300$ ohms. Other system parameters were $T = 1.22$ μs, $C = 5$ nF, $L = 2$ mH, $R_{dac} = 1000$ ohms, and $\tau = 1.22$ μs. Poles are represented by "X" and zeros by "O". Rs=50.

with the system stable when $R_{ser} < 200$ ohms and unstable when $R_{ser} > 200$ ohms.

The root locus for the positive RLC case is shown in Fig. 3, where the capacitance is $C = 5$ nF, the inductance as $L = 2$ mH, and the remaining parameters were unchanged. R_{ser} is varied from $R_{ser} = -300$ ohms to $R_{ser} = 500$ ohms in steps of 100 ohms. For the positive RLC case, the edge of stability occurred at $R_{ser} \approx -300$ ohms with system stable when $R_{ser} > -300$ ohms and unstable when $R_{ser} < -300$ ohms.

IV. Simulation Results

The digital discrete-time circuit of Fig. 1(b) was simulated in the Keysight ADS large-signal S-parameter simulator to determine the input impedance $Z_{in}(s)$ with $H(z) = H_{RLC}(z)$. The simulation was performed for both a negative RLC example and and a positive RLC example.

For the root-locus example of Fig. 2, simulation results are given in Fig. 4 for a digital negative RLC example with $C = -5$ nF, $L = -2$ mH, and $R_{ser} = 150$ ohms. Other system parameters were a DAC output resistance of $R_{dac} = 1000$ ohms, a period of $T = 1.22$ μs, and a latency $\tau = 1.22$ μs or one clock cycle. Simulation results are plotted along with theoretical input impedance from (1). In Fig. 4, the solid red curve and dotted blue curve represent the real and imaginary part of the theoretical input impedance Z_{in} respectively. The imaginary part of an ideal (R=0) *analog* negative LC is shown as the black dash-dotted curve. The real and imaginary parts of the simulated input impedance are represented by short-dash magenta and the long-dash cyan curve respectively. In Fig. 4, at $f \approx 40$ kHz, when the circuit is behaving as a negative capacitor, the theoretical input impedance is $Z_{in} = -217 + j270$ ohms compared with a simulated impedance of $Z_{in} = -145 + j304$ ohms. The positive reactance is associated with the negative capacitance of decreasing magnitude as the frequency increases. At $f \approx 60$ kHz, when the circuit is behaving as a negative inductor, the theoretical input impedance is $Z_{in} = 188 - j304$ ohms compared with a simulated impedance of $Z_{in} = 170 - j372$ ohms. The negative reactance is associated with the negative inductance of increasing magnitude as the frequency increases.

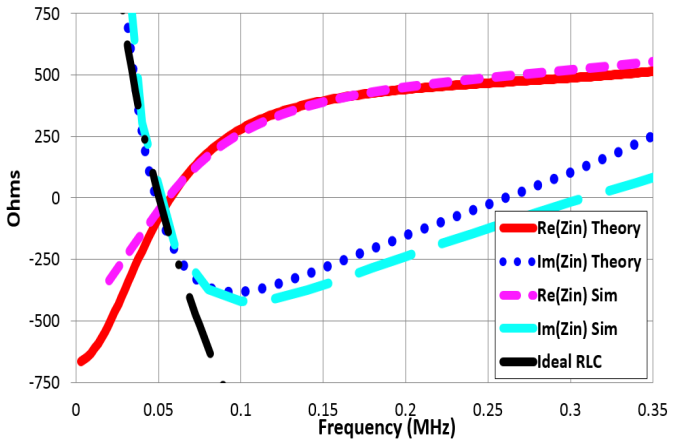

Fig. 4. Simulation results for the negative RLC circuit of Fig. 1 versus theoretical results calculated from equation (1) when $H(z) = H_{RLC}$. The system parameters are $T = 1.22$ μs, $C = -5$ nF, $L = -2$ mH, $R_{ser} = 150$ ohms, $R_{dac} = 1000$ ohms, and $\tau = 1.22$ μs. Solid red curve is theoretical $Re(Z_{in})$, short-dash magenta is simulated $Re(Z_{in})$, dotted-blue curve is theoretical $Im(Z_{in})$, long-dash cyan is simulated $Im(Z_{in})$, and black dash-dotted curve is ideal $Im(Z_{in})$.

For the root-locus example of Fig. 3, simulation results are given in in Fig. 5 for a digital positive RLC example with $C = 5$ nF, $L = 2$ mH, and $R_{ser} = -150$ ohms, and all other system parameters the same as the negative RLC. Simulation results are again plotted along with theoretical input impedance from (1), with real and imaginary parts of Z_{in} plotted in solid red curve and dotted blue respectively for theory, and plotted in short-dash magenta and the long-dash cyan respectively for

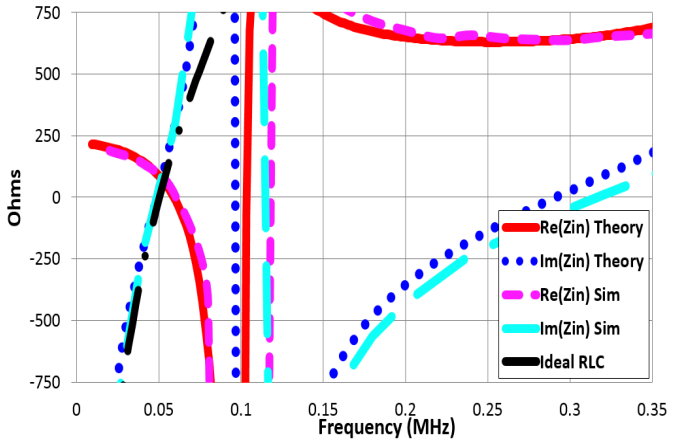

Fig. 5. Simulation results for the positive RLC circuit of Fig. 1 versus theoretical results calculated from equation (1) when $H(z) = H_{RLC}$. The system parameters are $T = 1.22$ μs, $C = 5$ nF, $L = 2$ mH, $R_{ser} = -150$ ohms, $R_{dac} = 1000$ ohms, and $\tau = 1.22$ μs. Solid red curve is theoretical $Re(Z_{in})$, short-dash magenta is simulated $Re(Z_{in})$, dotted-blue curve is theoretical $Im(Z_{in})$, long-dash cyan is simulated $Im(Z_{in})$, and black dash-dotted curve is ideal $Im(Z_{in})$.

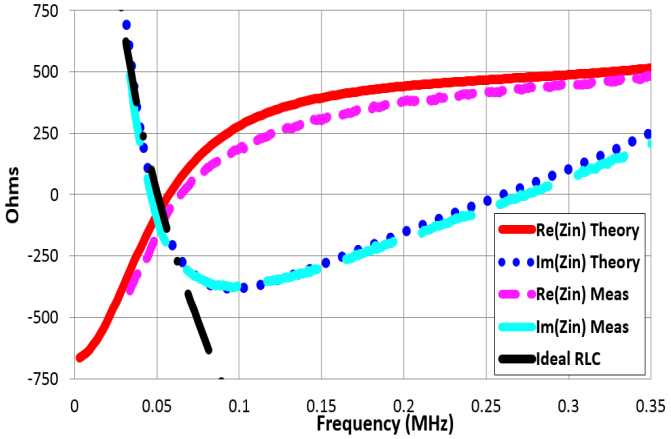

Fig. 6. Measurement results for the negative RLC circuit of Fig. 1 versus theoretical results calculated from equation (1) when $H(z) = H_{RLC}$. The system parameters are $T = 1.22$ μs, $C = -5$ nF, $L = -2$ mH, $R_{ser} = 150$ ohms, $R_{dac} = 1000$ ohms, and $\tau = 1.22$ μs. Solid red curve is theoretical $Re(Z_{in})$, short-dash magenta is simulated $Re(Z_{in})$, dotted-blue curve is theoretical $Im(Z_{in})$, long-dash cyan is simulated $Im(Z_{in})$, and black dash-dotted curve is ideal $Im(Z_{in})$.

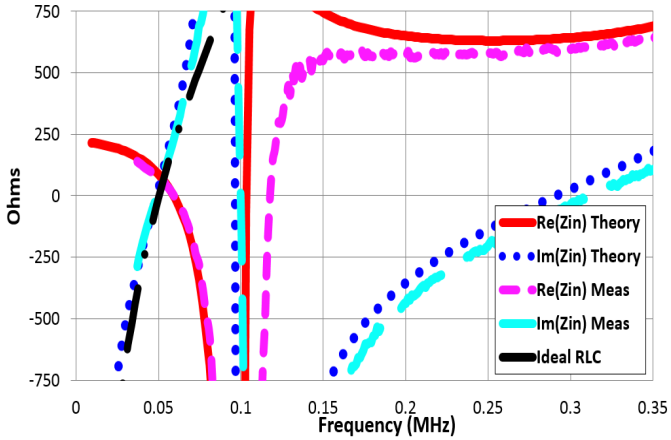

Fig. 7. Measurement results for the positive RLC circuit of Fig. 1 versus theoretical results calculated from equation (1) when $H(z) = H_{RLC}$. The system parameters are $T = 1.22$ μs, $C = 5$ nF, $L = 2$ mH, $R_{ser} = -150$ ohms, $R_{dac} = 1000$ ohms, and $\tau = 1.22$ μs. Solid red curve is theoretical $Re(Z_{in})$, short-dash magenta is simulated $Re(Z_{in})$, dotted-blue curve is theoretical $Im(Z_{in})$, long-dash cyan is simulated $Im(Z_{in})$, and black dash-dotted curve is ideal $Im(Z_{in})$.

the simulation. The imaginary part of an ideal (R=0) *analog* positive LC is shown as the black dash-dotted curve. In Fig. 5, at $f \approx 40$ kHz, when the circuit is behaving as a positive capacitor, the theoretical input impedance is $Z_{in} = 146 - j226$ ohms compared with a simulated impedance of $Z_{in} = 139 - j229$ ohms. At $f \approx 60$ kHz, when the circuit is behaving as a positive inductor, the theoretical input impedance is $Z_{in} = -14 + j313$ ohms compared with a simulated impedance of $Z_{in} = 6 + j296$ ohms.

V. Prototype and Measurements

The system of Fig. 1 was prototyped using the NXP FRDM-K64F development board. The board features an on board 16-bit ADC and 12-bit DAC. To implement the series RLC circuit, H_{RLC} from (4) was programmed onto the board for both the negative RLC circuit, with negative L and negative C, and the positive RLC circuit, with positive L and positive C. Parameters common to both cases were $R_{dac} = 1000$ ohms, $\tau = 1.22$ μs, and $T = 1.22$ μs. The period T was determined as a result of the achievable computation time and ADC clock frequency for the the NXP FRDM-K64F board, with a final effective sampling rate of approx. 0.82 MHz.

Measurements for the negative RLC circuit ($C = -5$ nF, $L = -2$ mH, $R_{ser} = 150$ Ω) and positive RLC circuit ($C = 5$ nF, $L = 2$ mH, $R_{ser} = -150$ Ω) are shown in Fig. 6 and Fig. 7 respectively, along with the predicted theoretical input impedance Z_{in} from (1). In both figures the solid red curve is the real part of theoretical input impedance, and the short-dash magenta curve is the real part of the simulated input impedance. The dotted blue curve is the imaginary part of the theoretical input impedance, and the long-dash cyan curve is the imaginary part of the simulated input impedance. The imaginary part of an ideal (R=0) *analog* negative LC is shown as the black dash-dotted curve.

The digital discrete time negative RLC circuit measurements in Fig. 6 were for a capacitance $C = -5$ nF, an inductance of $L = -2$ mH, and a series resistance of $R_{ser} = 150$ ohms. At $f \approx 38$ kHz the theoretical input impedance is $Z_{in} = -247 + j358$ ohms compared with a measured impedance of $Z_{in} = -355 + j321$ ohms. At $f \approx 53$ kHz the theoretical input impedance is $Z_{in} = -34 - j127$ ohms compared with a measured impedance of $Z_{in} = -135 - j151$ ohms.

The digital discrete time positive RLC circuit measurements in Fig. 7 were for a capacitance of $C = 5$ nF, an inductance of $L = 2$ mH, and a series resistance of $R_{ser} = -150$ ohms. At $f \approx 44$ kHz the theoretical input impedance is $Z_{in} = 126 - j120$ ohms compared with a measured impedance of $Z_{in} = 104 - j104$ ohms. At $f \approx 52$ kHz the theoretical input impedance is $Z_{in} = 71 + j87$ ohms compared with a measured impedance of $Z_{in} = 66 + j82$ ohms. The prototype system of Fig. 1 using the NXP FRDM-K64F development board is shown in Fig. 8.

VI. Conclusion

A digital negative RLC circuit, with negative inductance and negative capacitance, and a digital positive RLC circuit, with positive inductance and positive capacitance, were presented. Stable regions of operation were determined using stability conditions and a root locus analysis. Simulation and measurement results were in agreement with theory for both the digital negative RLC and digital positive RLC cases.

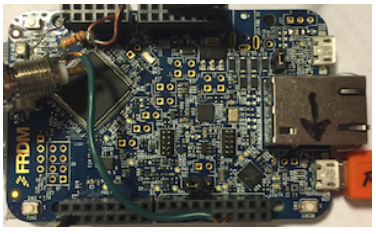

Fig. 8. NXP FRDM-K64F development board prototype.

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