Capacitance and Bandwidth Tradeoffs in a Cross-Coupled CMOS Negative Capacitor

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***Abstract*—Recent advances in technology have driven renewed interest in the design of CMOS negative capacitance circuits for diverse applications such as wideband metamaterials and radio frequency integrated circuits. In practice, the particular CMOS fabrication process generally limits the practical range of capacitance values and bandwidths that can be achieved. In addition, the reactive component of the desired impedance is often accompanied by a parasitic resistive component. To address these issues, a CMOS cross-coupled negative capacitance circuit is designed and simulated in a 0.5 micron CMOS process. Results are presented for -5 pF, -10 pF, and -20 pF designs with ten-percent bandwidths of approximately 140 MHz, 100 MHz, and 80 MHz respectively.**

Keywords—negative capacitance; negative impedance converter; CMOS; integrated circuit.

I. INTRODUCTION

Recent interest in the development of integrated circuits that exhibit negative capacitance is driven by a number of emerging applications. In metamaterial applications, negative capacitance is used to provide wideband performance in otherwise narrowband structures [1], [11]-[12]. In radio receiver applications, negative capacitance is used to provide wideband performance in radio receiver front ends [2]. In antenna matching, negative capacitance can be used to achieve broadband, electrically-small antennas [3]-[5].

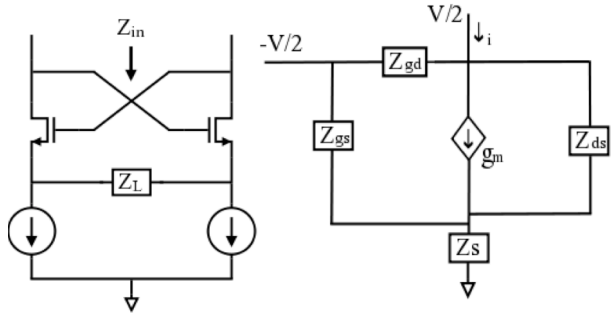
To address these emerging needs, a CMOS cross-coupled negative capacitance circuit is designed and simulated in a 0.5 micron CMOS process [6]-[10]. A cross-coupled negative capacitance circuit is chosen because it provides a differential input as opposed to a single-ended grounded configuration. Although more advanced processes may offer increased bandwidth, a 0.5 micron CMOS process offers the advantages of lower cost and a 5 volt power supply to support larger voltage signals. In addition, the bandwidth of negative capacitance circuits is expected to decrease as the magnitude of the negative capacitance is increased. Therefore, the present article investigates tradeoffs of capacitance and bandwidth.

The proposed CMOS cross-coupled negative capacitor design consists of a pair of cross-coupled transistors with supporting bias circuits [6]-[10]. This basic circuit is a Negative Impedance Converter (NIC) that converts the impedance of a load reactance. Ideally, this circuit should convert a differential capacitive load into a differential negative capacitance. However, analysis of the circuit shows that the desired negative capacitance is accompanied by an undesired negative resistance component that is inversely proportional to the transconductance of the cross-coupled transistors. Therefore, a diode-connected transistor is also proposed to be added in series with the cross-coupled output to reduce the aforementioned negative resistance component.

In the next section, the analysis of the basic cross-coupled circuit is first presented, including the expected parasitic resistance. The subsequent section describes the detailed design and layout of the proposed circuit, and the final section provides simulation results that demonstrate performance tradeoffs between bandwidth and negative capacitance value.

II. CIRCUIT ANALYSIS

The basic cross-coupled CMOS circuit is shown in Fig. 1(a) and functions as a negative impedance converter, where the load impedance Z_L is converted to negative impedance Z_{in}. Also, the analysis model for the left half of the circuit in Fig. 1(a) is shown in Fig. 1(b). As shown in Fig. 1(a), the basic circuit is comprised of two cross-coupled nMOS transistors, where the gates of each device are connected to the



(a) (b)

Fig. 1. Left-hand circuit (a) above shows the basic cross-coupled circuit for analysis purposes [7], and the right-hand circuit (b) shows the analysis model for the left half of the basic circuit in (a).

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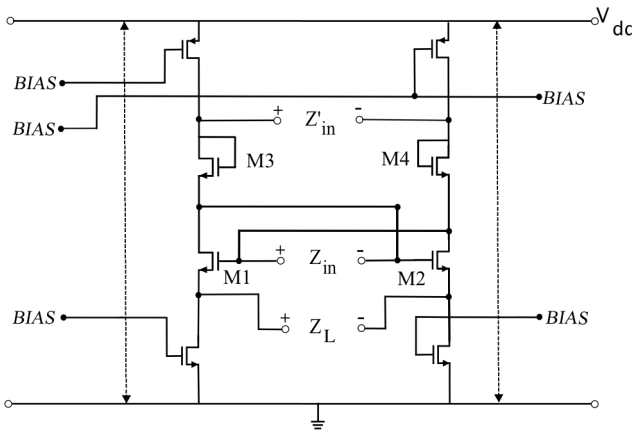

Fig. 2. Detailed schematic of cross-coupled circuit.

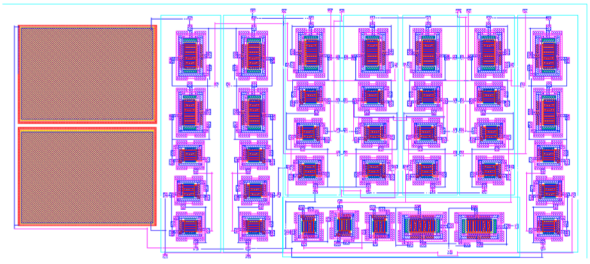

Fig. 3. Layout of cross-coupled negative capacitance circuit in 0.5 micron CMOS with biasing shown.

drains of the opposite device. Two current sources provide identical current to each device, and the load is connected across the sources of the cross-coupled pair.

To begin analysis of the circuit of Fig. 1, the current at the drain of each device is:

$$i_d = \frac{V_{in}}{Z_{gd}} + g_m\left(-\frac{V_{in}}{2} - v_s\right) + \frac{V_{in}/2 - V_s}{Z_{ds}}, \quad (1)$$

where i_d is drain current, v_{in} is the differential input voltage seen at Z_{in} of Fig. 1(a) and denoted V in Fig. 1(b), v_s is the source voltage, z_{gd} is the gate-drain impedance, g_m is the transconductance, and z_{ds} is the drain-source impedance of M1 and M2 for the corresponding half-circuit in Fig. 1(b).

The current at the source is:

$$i_s = \frac{v_s}{Z_s} = \frac{-v_{in}/2 - v_s}{Z_{gs}} + g_m\left(-\frac{v_{in}}{2} - v_s\right) + \frac{v_{in}/2 - v_s}{Z_{ds}}, \quad (2)$$

where $z_s = Z_L/2$ for the half-circuit, and z_{ds} is the drain-source impedance of M1 and M2. After solving for i_d and i_s, the input admittance $Y_{in} = 1/Z_{in}$ of the circuit is obtained as

$$Y_{in} = \left(y_{gd} - \frac{g_m}{2} + \frac{y_{ds}}{2}\right) - \frac{(y_{ds} - g_m - y_{gs})(g_m + y_{ds})}{2(y_s + y_{gs} + g_m + y_{ds})}. \quad (3)$$

Considering the case for $y_s + g_m >> y_{gs} + y_{ds}$ and $g_m >> y_{gd} + y_{ds}$, and solving the above equation, gives input admittance

$$Y_{in} \approx -\frac{1}{2}\left(\frac{g_m y_s}{g_m + y_s}\right), \quad (4)$$

and corresponding input impedance is

$$Z_{in} \approx -2z_s - \frac{2}{g_m} = -Z_L - \frac{2}{g_m}. \quad (5)$$

For the input impedance at the point Z'_{in} of Fig. 2 that includes the additional pair of diode-connected transistor impedances in series with Z_{in}, the total impedance becomes

$$Z'_{in} \approx -Z_L - \frac{2}{g_m} + \frac{2}{g_{m3}}, \quad (6)$$

where diode-connected devices M3 and M4 have transconductance g_{m3}.

III. Simulation Results

The detailed schematic of the cross-coupled NIC is shown in Fig. 2, where M1 and M2 form the cross-coupled nMOS transistor pair corresponding to the simplified circuit of Fig. 1, with dimensions 50×0.5 microns. Transistors M3 and M4 comprise the diode compensation. Bias is set on both sides, where all pMOS are 100×0.5 microns and nMOS are 50×0.5 microns. The layout of the proposed design in 0.5 micron CMOS is shown in Fig. 3, and S-parameters in Fig. 4. The design is currently out for fabrication.

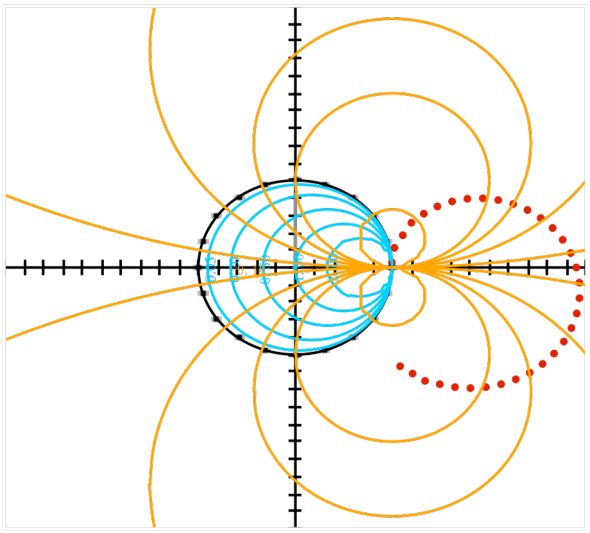

Fig. 4. Smith chart for S_{11} (dotted red) corresponding to Z'_{in}. This plot is observed outside the normal Smith chart regions due to the negative resistance.

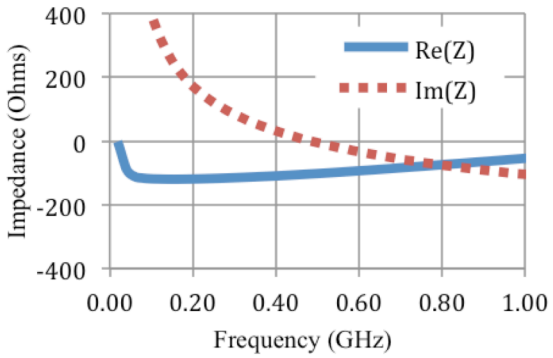

Fig. 5. Simulation results showing real part of Z'_{in} (solid blue) and imaginary part of Z'_{in} (dotted red) for a 5 pF capacitive load.

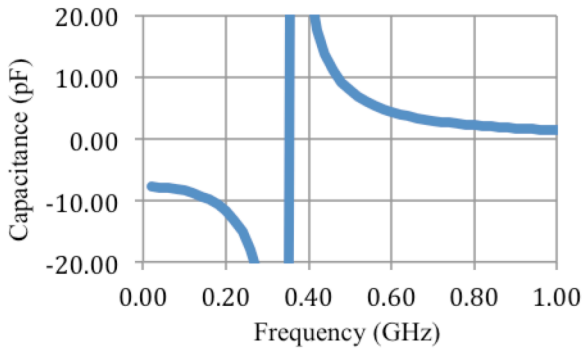

Fig. 7. Simulation results showing input capacitance observed at Z'_{in} for a load capacitance Z_L of 10 pF (computed capacitance values above the resonance near 380 MHz are anomalous due to zero crossing of Im(Z)).

First, the design was evaluated with a 5 pF on-chip load for Z_L to test the bandwidth of a -5 pF negative capacitance. A plot of S_{11} for the device is shown in Fig. 4, where the performance is observed outside the normal Smith chart regions due to the negative resistance. The real and imaginary parts of Z_{in} are shown in Fig. 5 for the 5 pF capacitive load, with simulation results showing the real part of Z_{in} in ohms (solid blue) and imaginary part of Z_{in} in ohms (dotted red). As it can be seen, the reactance is that of a negative capacitance, where the sign of the imaginary part of Z_{in} is inverted from that of a positive capacitance. Also, the diode-connected compensation scheme results in the magnitude of observed negative resistance being kept below 100 ohms, as shown in the solid blue curve of Fig. 5.

The negative capacitance plots for Z_{in} are shown in Figs. 6, 7, and 8 for the respective on-chip loads of 5 pF, 10 pF and 20 pF. These plots show corresponding low-frequency capacitances of -3.8 pF, -7.8 pF, and -15.8 pF respectively at low frequency. Also, note that the computed capacitance values at frequencies above the resonances are anomalous artifacts of the computation. These anomalous values occur due to the zero crossing of Im(Z) in the figures. Nevertheless, the low-frequency negative capacitance values in Figs. 6, 7, and 8 correspond well with the predicted capacitance values of -5 pF, -10 pF, and -20 pF using the approximation in (6).

From the simulation results shown in Fig. 6, the input capacitance is -3.8 pF at low frequencies when the NIC is loaded with a 5 pF capacitor. The input capacitance remains within 10 percent up to 140 MHz, and within 20 percent up to 190 MHz. Similarly, the simulation results of Fig. 7 indicate a low-frequency input capacitance of -7.8 pF when the NIC is loaded with a 10 pF capacitor. Here, the input capacitance remains within 10 percent up to 100 MHz, and within 20 percent up to 150 MHz. The simulation results shown in Fig. 8 indicate a low-frequency input capacitance of -15.8 pF when the NIC is loaded with a 20 pF capacitor. Here, the input capacitance remains within 10 percent up to 80 MHz, and within 20 percent up to 100 MHz.

IV. Conclusion

A cross-coupled negative capacitance circuit was designed and simulated for different loads of 5 pF, 10 pF, and 20 pF.

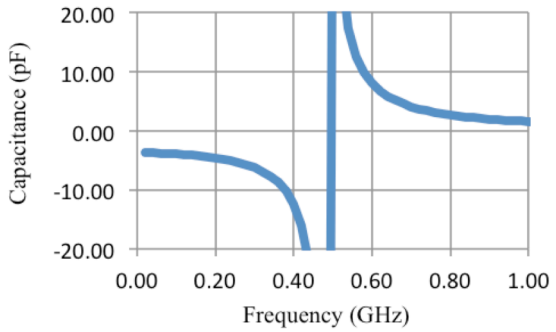

Fig. 6. Simulation results showing input capacitance observed at Z'_{in} for a load capacitance Z_L of 5 pF (computed capacitance values above the resonance near 500 MHz are anomalous due to zero crossing of Im(Z) in Fig. 5).

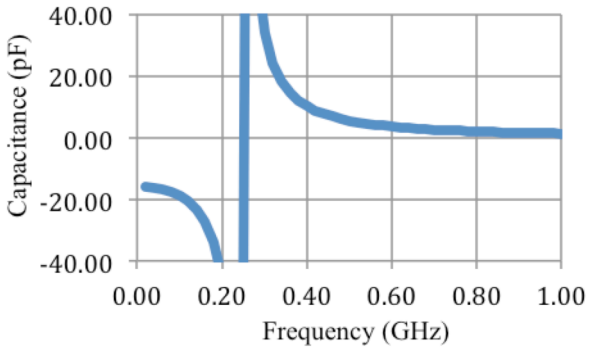

Fig. 8. Simulation results showing input capacitance observed at Z'_{in} for a load capacitance Z_L of 20 pF (computed capacitance values above the resonance near 250 MHz are anomalous due to zero crossing of Im(Z)).

The analysis of the circuit, under simplifying assumptions, shows that the expected observed capacitance should approximately equal the negative of the load capacitance. The simulation results are in good agreement with derived approximations, where the observed capacitances were -3.8 pF, -7.8 pF, and -15.8 pF. These simulation results include the presence of series diode-connected transistors used to reduce a parasitic negative resistance inherent in the basic circuit. The analysis shows that this undesired series parasitic negative resistance is inversely proportional to the transconductance of the cross-coupled transistors. With the proposed diode-connected compensation scheme, the magnitude of observed negative resistance is kept below 100 ohms. In addition, results are presented that show the variation in the bandwidth of cross-coupled negative capacitance circuits as the magnitude of the negative capacitance is increased.

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