# Single Chip Spectrum Sensing Module in CMOS with Digital Frequency Synthesizer and Digital Output

Raghu K. Mulagada, Yi Yang, Thomas P. Weldon, and Don T. Lieu
Department of Electrical and Computer Engineering
University of North Carolina at Charlotte
Charlotte, NC, USA.
tpweldon@uncc.edu

*Abstract* — **In a congested wireless environment, an increasing number of applications require the capability to measure frequency spectrum. This motivates the development of a spectrum-sensing module comprised of a minimal architecture spectrum analyzer with integrated frequency synthesized tuning. The module features a frequency synthesizer with digital frequency controlled inputs and an integrated analog-to-digital converter to digitize the output. This module can be incorporated as a basic component in more complex system that require spectral sensing such as spectrum monitoring systems and dynamic spectrum access systems. The proposed single-chip spectrum-sensing module with digital output was fabricated in a standard 0.5 micron CMOS process. Measured results of a prototype are presented for operating range of 20 to 180 MHz.**

***Keywords - Cognitive Radio, Spectral Information, Frequency Sythesizer, Log Amplifier, Successive Approximation ADC.***

## I. INTRODUCTION

In traditional spectrum allocation, radios were allowed to operate only within a band of frequencies allocated or licensed for their specific usage. However, with the evolution of wireless communication and introduction of new protocols, spectral resources are quickly exhausted. This motivated research into effective utilization of the available spectrum. The inefficient usage of the licensed spectrum [1] prompted the development of spectral monitoring and Dynamic Spectrum Access (DSA) systems [2]-[6]. The premise of these technologies is to improve spectral efficiency by allowing Secondary Users (SU) to utilize a band allocated to a Primary User (PU) in an opportunistic manner. An important factor in implementing these systems is the need to characterize the local frequency spectrum, and this motivates the present investigation of a simple single-chip spectrum analyzer. Cognitive Radio (CR) systems and Software Defined Radio (SDR) systems are few proposed approaches to implement dynamic spectrum access. Nevertheless, based on experimental measurements in [2], it can be argued that the proposed spectrum analyzer is amenable to a variety of applications.

There are different architectures for realizing a spectrum analyzer that have been reported in literature [8]-[10]. Each of those is built around diverse platforms and serves a distinct purpose. The speech spectrum analyzer in [8] is based on monolithic switched capacitor implementation and has a limited bandwidth. The real time RF spectrum analyzer reported in [10] uses surface-acoustic-wave devices which make it harder to implement a CMOS counterpart. Most signal processing approaches to realizing a spectrum analyzer are similar to [9], in that the RF signal is converted using an Analog to Digital Converter (ADC) and Fast Fourier Transform (FFT) is applied on the resulting digitized signal to glean spectral information. This technique not only requires high resolution ADCs with high sampling rates [13], but also fast memory, and FFT hardware or off-line FFT processing [9]. These performance requirements might be reasonable for a base station, but are at premium for a mobile terminal with spectrum sensing capabilities as they lack the power and computational capabilities to perform those tasks. Therefore, the proposed design approach for high-frequency spectral estimation is distinct from those prior spectrum analyzer approaches. Furthermore, the present approach appears to be the first fully integrated, CMOS, non-FFT spectrum analyzer in the literature with digital input frequency tuning, digital output, and operating at frequencies up to 200 MHz.

The development of the proposed single-chip frequency-synthesized digital spectrum analyzer is undertaken to address limitations of aforementioned systems. Detection of spectrum usage using the proposed system should result in reduced complexity and power consumption. To achieve such goals, a simple ac-coupled zero intermediate frequency (zero-IF) system is chosen. The spectral information is presented as a digitized logarithmic video output. The digitization of the output is done using an ADC with low resolution running at moderate sampling frequencies. An on-chip frequency synthesizer provides the necessary frequency accuracy. The system presented here is minimal complexity architecture and hence has limited capabilities in terms of performance and controllability. However, it should be noted that a more complicated architecture based on this platform and additional features could potentially lead to improved performance and controllability. Results from experiments conducted on a prototype of the proposed system provide insight into the baseline capability of an elementary spectrum analyzer. Implementation of the proposed system in CMOS and the digitization of the output make it a good candidate for integration into larger and more complex systems.

This paper is organized as following. In section II, designs of the proposed digital spectrum analyzer and on-chip frequency synthesizer are described. In section III, measured data from experiments conducted on a prototype system,

fabricated in standard 0.5 micron CMOS process are presented. Finally, conclusions are drawn in section IV.

## II. ARCHITECTURE

A form energy detection, wherein the signal strength detection capability of a logarithmic amplifier is exploited for spectrum sensing, provided the starting point for designing the proposed module. The sensed spectrum is presented as a logarithmic video output. This output can be calibrated based on system characteristics to yield spectral information in terms of frequency of the sensed signal and power contained in it at the location of measurement. These signal detection capabilities are inherent to the sensing module and hence eliminate the need for computations such as FFT.

To further minimize complexity of the proposed system and reduce hardware requirements, an ac-coupled zero-IF architecture was selected for the proposed single-chip digital spectrum analyzer integrated circuit. An important aspect of zero-IF method that made it the design of choice is absence of filters, which would have otherwise been required for the purposes of image rejection and IF signal conditioning. A design trade-off is necessitated to address the issue of dc-offset in system. The ac-coupling method used for this purpose results in a small deadband near center frequency. The problematic deadband can be eliminated by frequency sweep adjustment or local oscillator frequency dithering. Frequency accuracy in the system is provided by an on-chip basic frequency synthesizer that is included in the design.

For sake of simplicity, the functioning of the proposed single-chip digital spectrum analyzer is explained based on a block diagram shown in Fig. 1. The Log Downconverter that forms the core of the spectrum analyzer and the Frequency Synthesizer which provides frequency accuracy are marked as individual sections. Each block is a functional depiction of one of the critical constituent components of their respective sections.

### *A. Frequency Synthesizer*

The purpose of Frequency Synthesizer, shown in upper section of Fig. 1, is to generate a local oscillator (LO) signal that can later be used for down-conversion. The frequency synthesizer has a divide by N block in its feedback loop that can be used for tuning. The frequency divider ratio N is set by an 8-bit wide parallel input bus (Freq. Set), one end of which is connected to a binary counter. A change of state in binary counter results in tuning the frequency by one step of 1.56 MHz. Speed of frequency tuning can be set externally by adjusting the RC time constant on the binary counter. Output signal from frequency divider drive one of the inputs of a phase frequency detector (PFD). A frequency reference (Ref. Freq. In) is fed to the other input of PFD. The PFD detects difference in phase between its two inputs signals and produces a proportional voltage. Output signal of the PFD is fed to a loop filter (LF) which assists in frequency pull-in and conditioning. The output of LP drives a voltage-controlled oscillator (VCO). Frequency of the output signal of VCO is proportional to applied voltage which in turn reflects the difference in phase between this signal and reference signal. The VCO output signal is fed back to the frequency divider to complete the negative feedback loop. A take away point from this signal drives the local oscillator port of the mixer in the Log Downconverter section.

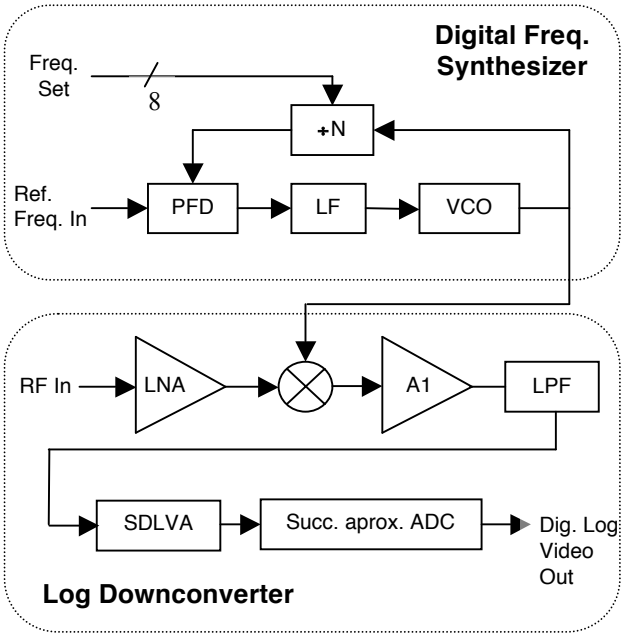


Fig. 1. Block diagram of the proposed single chip Spectrum Analyzer with frequency synthesized tuning. Spectrum Analyzer and Frequency Synthesizer blocks are marked for clarity.

### *B. Log Downconverter*

The Log Downconverter section, shown at bottom of Fig. 1, forms the core of the proposed digital spectrum analyzer system. A low noise amplifier (LNA) functions as front end of the proposed system and amplifies an incoming radio frequency input (RF In) signal. One of the terminals of Gilbert cell mixer used for down-conversion is driven by the amplified RF signal while the other terminal is driven by the output signal of VCO from frequency synthesizer. The IF output produced by mixer is amplified in an ac-coupled amplifier (A1). The amplified IF signal is then low-pass filtered and fed to the core of detection module, the successive-detection log video amplifier (SDLVA). Response of the SDLVA to an incident signal is a dc voltage that can be treated as a piece wise linear function of the logarithm of power level of that signal [11]. Finally, the video output voltage from SDLVA representing the spectrum is digitized using an 8-bit successive approximation ADC at a sampling frequency of about 1 MHz.

## III. EXPERIMENTAL RESULTS

A prototype of the proposed digital spectrum analyzer design was implemented in a standard 0.5 micron CMOS process, a photograph of which in Fig. 2. The major building blocks of the proposed system are marked with bounding boxes with details explained in the caption. A series of experiments were conducted using the prototype to assess its performance and characterize its behavior.

First, the logarithmic response of the spectrum analyzer was calibrated using an RF input signal at 100 MHz and is shown in Fig. 3. This calibration curve is an important characteristic of the system and is used to convert the

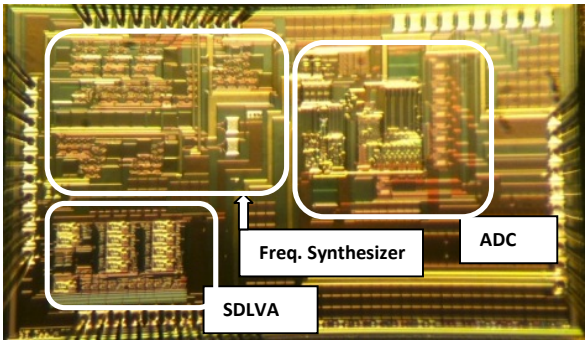


Fig. 2. Photograph of single-chip spectrum analyzer; lower box on left side surrounds frequency synthesizer, upper box on left side surrounds remainder of spectrum analyzer and box on right surrounds the successive approximation ADC.

logarithmic output voltages back into equivalent RF input power. It can be observed from fig. 3 that the relationship between RF input power and logarithmic output voltage is nearly linear for entire dynamic range of operation. An RF signal level of -5 dBm corresponds to an SDLVA output of approx. 20 mV, an RF signal level of -45 dBm corresponds to an SDLVA output of approx. 82 m, etc..

RF signals with incremental increase in frequency are used to test for the band in which the prototype can be operated with acceptable level of performance. For this initial testing, the ADC is not connected to a source and hence is not active. Since all of the measured data cannot be reproduced here, results from measurements at lowest operating frequency, an intermediate operating frequency and the highest operating frequency are presented. It is deemed that this data should be sufficient to infer the band of operation of the proposed system. Results from these measurements are shown in Fig. 4, Fig. 5 and Fig. 6 for a RF input signal of -10 dBm at 20 MHz, 100 MHz and 180 MHz respectively. In each of these figures, the upper oscilloscope trace is the logarithmic video output voltage of the spectrum analyzer chip as the frequency synthesizer varies from 1.56 MHz to 200 MHz in 128 steps. The lower trace in Figs. 4 – 6 shows the most significant bit of the Freq. Set input bus of Fig. 1. The falling edge of the lower trace is where the frequency synthesizer makes the transition from 200 MHz to 1.56 MHz, and at the rising edge of the lower trace is where the frequency synthesizer is set to 100 MHz.

The logarithmic video output is inverted for the particular SDLVA design that was used in the system. Therefore, the upper traces are an inverted version of the spectrum. So, lower voltages in upper traces indicate stronger signals. A spectral

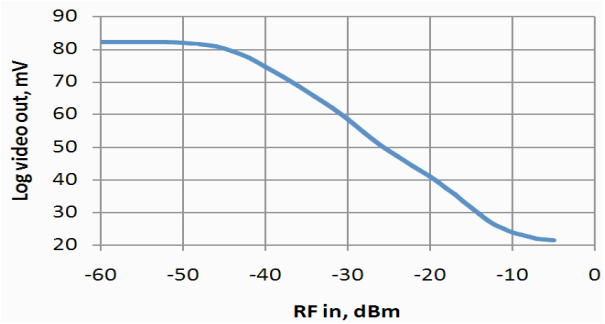


Fig. 3. Spectrum Analyzer response to a 100 MHz RF input signal. Horizontal axis is RF input power; vertical axis is logarithmic video output.

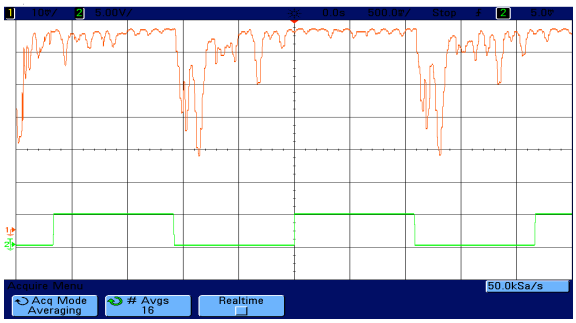


Fig. 4. Spectrum analyzer: measured spectrum of a 20 MHz, -10 dBm sinusoid. Horizontal axis is RF input frequency. Upper trace vertical axis is logarithmic video output voltage, at 10 mV/div. Bottom trace: falling edge indicates frequency synthesizer transition from 200 MHz to 1.56 MHz, rising edge indicates 100 MHz. Large dip in upper trace indicates strong 20 MHz RF input signal. Lower voltages indicate stronger signals.

peak corresponding to the input signal can be observed when the frequency synthesizer sweeps through that particular frequency. Response of the system to each of input frequencies is explained below the respective figure.

It can be observed form the measured spectral responses that there are various spurious responses present throughout the spectrum. The spurs to the right of observed peaks are due to instances when the frequency of LO signal matches with that of a harmonic of the input signal. The spurs at LO - 2RF, LO - 3RF are examples of such mixer spurious response. Spurs to left of observed peaks are sub-harmonic responses below the frequency of input signal are also due to various spurious responses of the mixer. The spurs at 2LO - RF spur and 3LO - RF are examples of such response. It should be noted that the spurious responses of the system are predictable and can probably be properly treated to get a cleaner response. One way to reduce spurs is to remove the harmonics of input signal using pre-selection filters or a band-limited antenna.

A two-tone RF input signal with strength of -10 dBm at 100 MHz was used to test for the frequency selectivity of the prototype. The separation between the tones is gradually increased until a perceptible difference separating the two measured tones is observed. Results of the preceding experiment are presented in Fig. 7. The measured sensitivity of the prototype is 10 MHz. The sensitivity of the system is a function of the quality factor of the LPF in Downconverter section, which unfortunately is not tunable. A tunable filter for

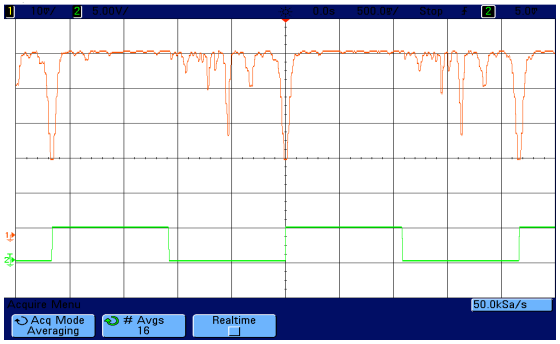


Fig. 5. Spectrum analyzer: measured spectrum of a -10 dBm 100 MHz sinusoid. Horizontal axis is RF input frequency. Upper trace vertical axis is logarithmic video output voltage, at 10 mV/div. Bottom trace: falling edge indicates frequency synthesizer transition from 200 MHz to 1.56 MHz, rising edge indicates 100 MHz. Large dip in upper trace indicates strong 100 MHz RF input signal. Lower voltages indicate stronger signals.

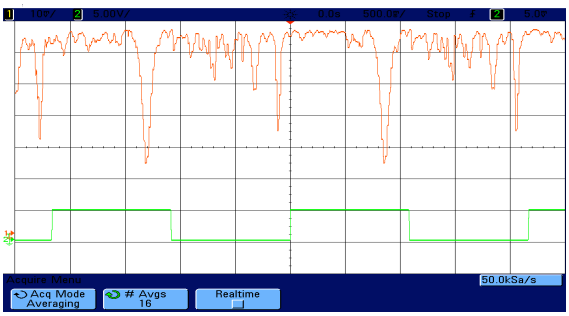


Fig. 6. Spectrum analyzer: measured spectrum of a 180 MHz, -10 dBm sinusoid. Horizontal axis is RF input frequency. Upper trace vertical axis is logarithmic video output voltage, at 10 mV/div. Bottom trace: falling edge indicates frequency synthesizer transition from 200 MHz to 0 Hz, rising edge indicates 100 MHz. Large dip in upper trace indicates strong 180 MHz RF input signal. Lower voltages indicate stronger signals.

LPF was not used to avoid any unnecessary complication.

Finally, the successive approximation ADC is connected into the system and spectrum measurements are made for an input RF signal of -10 dBm at 100 MHz. The digitized data from the ADC is analyzed using a custom MATLAB™ code to glean the spectral information. The resulting spectrum is shown in Fig. 8. It can be observed from Fig. 8 that the introduction of ADC into the system leads to increased noise and loss in finer details of the spectrum. This might be a reasonable trade-off owing to the ease of integration provided by the digital output.

## IV. Conclusion

A prototype of single-chip frequency-synthesized digital spectrum analyzer with digital output has been fabricated in 0.5 micron CMOS. Test results were presented to demonstrate its operation from 20 MHz to 200 MHz. Though the minimal architecture limits its performance, the prototype integrated circuit demonstrates baseline capabilities of the proposed simple spectrum analyzer architecture.

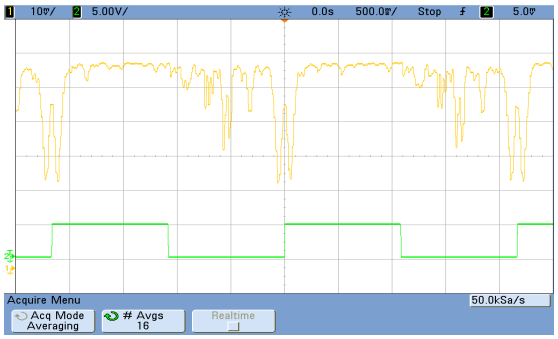


Fig. 7. Spectrum analyzer: measured spectrum of a -10 dBm two-tone 100 MHz sinusoid. The two tones are separated by 10 MHz in frequency. Horizontal axis is RF input frequency. Upper trace vertical axis is logarithmic video output voltage, at 10 mV/div. Bottom trace: falling edge indicates frequency synthesizer transition from 200 MHz to 1.56 MHz, rising edge indicates 100 MHz. Large dip in upper trace indicates strong two-tone 100 MHz RF input signal. Output is inverted, where lower voltages indicate stronger signals.

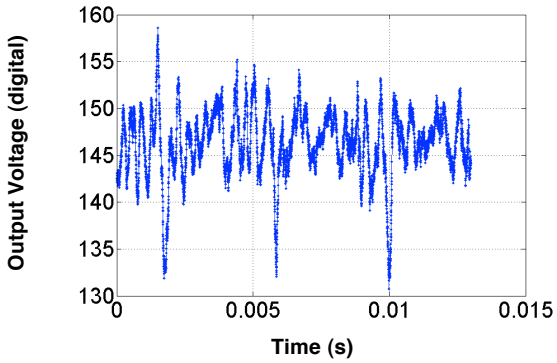


Fig. 8. Output of the spectrum sensing module in digital form. Input from signal generator is 100 MHz RF signal at a power level of -10 dBm.

## References

[1] FCC, *Spectrum Policy Task Force Report*, ET Docket No. 02-155, Nov. 2002.

[2] A.E.E. Rogers, J.C. Carter, M. Derome, and D.L. Smythe, "Extending the Dynamic Range of a Spectrum Monitor Using Comparison Switching and Spectral Averaging," *IEEE Trans. on Instrumentation and Measurement,* vol. 57, no. 3, pp. 591-594, March 2008.

[3] D. Boudreau, C. Dubuc, et al., "A fast automatic modulation recognition algorithm and its implementation in a spectrum monitoring application," *MILCOM 2000, 21st Century Military Communications Conference Proceedings*, vol. 2, pp. 732-736, 22-25 Oct. 2000.

[4] Qing Zhao and B.M. Sadler, "A survey of Dynamic Spectrum Access," *IEEE Signal Processing Magazine*, pp. 79-89, May 2007.

[5] G.J. Minden et al., "Cognitive radios for dynamic spectrum access - An Agile Radio for Wireless Innovation," *IEEE Communications Magazine*, pp. 113-121, May 2007.

[6] S. Geirhofer, Lang Tong, and B.M. Sadler, "Cognitive radios for dynamic spectrum access - Dynamic Spectrum Access in the Time Domain: Modeling and Exploiting White Space," *IEEE Communications Magazine*, pp. 66-72, May 2007.

[7] Ling Luo and S. Roy, "A Two-Stage Sensing Technique for Dynamic Spectrum Access," *IEEE International Conference on Communications*, pp. 4181-4185, 19-23 May 2008.

[8] J.S. Chang and Y.C Tong, "A micropower-compatible time-multiplexed SC speech spectrum analyzer design," *IEEE Journal of Solid-State Circuits*, vol. 28, no. 1, pp. 40-48, Jan. 1993.

[9] T. Sansaloni, A. Perez-Pascual, et al., "FFT Spectrum Analyzer Project for Teaching Digital Signal Processing With FPGA Devices," *IEEE Transactions on Education*, vol. 50, no. 3, pp. 229-235, Aug. 2007.

[10] D.W. Palmer, R.W. Brocato, et al., "Real-time RF spectrum analyzer: Components and system development," *Electronic Components and Technology Conference*, pp. 155-157, 27-30 May 2008.

[11] R.J. Baker, H.W. Li, D.E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, New York, Wiley-IEEE Press, 1997.

[12] K. Kimura, "A CMOS logarithmic IF amplifier with unbalanced source-coupled pairs," IEEE Journal of Solid-State Circuits, vol. 28, no. 1, pp. 78-83, Jan. 1993.

[13] Volker Blaschke, Tobias Renk, Friedrich K. Jondral, "A Cognitive Radio Receiver Supporting Wide-Band Sensing", *ICC workshop proceedings,*pp.499-503,2008.