Measurement of a Clock-Tuned Digital Non-Foster Circuit for Positive or Negative Digital Capacitance

Patrick J. Kehoe, Killian K. Steer, and Thomas P. Weldon
Department of Electrical and Computer Engineering
University of North Carolina at Charlotte
Charlotte, North Carolina 28223
Email: tpweldon@uncc.edu

***Abstract*—Theory and measured results are presented for a clock-tuned digital capacitor that provides digital implementation of a variable non-Foster negative capacitance or a variable positive capacitance. Unlike previous digital non-Foster capacitor designs, the proposed approach provides a variable capacitance without requiring changes to the signal processing hardware or embedded software. Instead, a single external clock provides simple control of the variable negative or positive capacitance of the circuit. Theoretical results are provided showing that predicted digital capacitance is inversely proportional to clock frequency, and associated parasitic resistance is determined by design parameters. Simulation results and prototype measurements confirm the underlying theory, and demonstrate the efficacy of the proposed approach.**

I. Introduction

There is renewed interest in exploiting non-Foster circuit elements such as negative capacitors and negative inductors to enhance performance in diverse applications such as artificial magnetic conductors, wideband metamaterials, software defined radios, and electrically-small antennas [1]–[4]. More recent digital implementations of non-Foster circuits afford potential advantages over analog approaches in providing accurate software-tunable capacitance [5]–[8]. Despite the advantages of digital non-Foster circuits, implementation of variable capacitance would require changing the signal processing hardware or embedded software. Therefore, a simple clock-tuned digital non-Foster circuit is proposed, to avoid the complexity of reconfiguring hardware or reprogramming software. In this, the frequency of an external digital clock establishes the digital capacitance.

The proposed approach for clock-tuned negative (or positive) digital capacitance builds upon previous implementations of digital non-Foster circuit elements in [6]. The approach is based on new theoretical analysis that shows that the effective capacitance of a digital capacitor is inversely proportional to the sampling rate. In addition, parasitic resistance is shown to be a function of design parameters and latency, and may therefore be adjusted as part of the design process.

In the following section, theory for the proposed clock-tuned digital capacitance circuit is presented. In the subsequent section, simulation results are compared with theoretical results. Finally, system stability and underlying theory are confirmed by measured data for a prototype.

978–1–5386–1539–3/17/$31.00 © 2017 IEEE

II. Theory

A block diagram of the proposed clock-tuned digital capacitor is shown in Fig. 1, following the approach in [6]. The clock signal clk with frequency $f_c = 1/T_c$ sets the ADC and DAC sample rates, with the ADC output being $v_{in}[n] = v_{in}(nT_c)$. Digital signal processing filter block $H(z)$ forms output $v_{dac}[n] = h[n] * v_{in}[n]$, which the DAC then converts to continuous-time voltage $v_{dac}(t)$. The DAC Thèvenin source impedance is R_{dac}, and latency associated with conversion time and processing time are modeled by time delay τ. Assuming a zero-order hold, the Laplace transform of $v_{dac}(t)$ becomes $V_{dac}(s) = V^\star(s)H(z)(1-z^{-1})e^{-s\tau}/s\big|_{z=e^{sT_c}}$, where $V^\star(s) = \sum v(nT_c)e^{-nsT_c}$ is the starred transform [9].

The input current to the circuit is then $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$. Solving for the input impedance $V_{in}(s)/I_{in}(s)$ results in the input impedance [6]

$$Z_{in}(s, f_c) \approx \left. \frac{s\ R_{dac}/f_c}{s/f_c - H(z)(1-z^{-1})e^{-s\tau}} \right|_{z=e^{s/f_c}} . \qquad (1)$$

Next, consider a simple RC circuit with capacitance C_0, and series resistance R_{ser}, at an initial sampling period of T_0. Here, $v(t) = \int i(t)dt/C_0 + i(t)R_{ser}$. Differentiating yields, $dv(t)/dt = i(t)/C_0 + R_{ser}di_{in}(t)/dt$. Now, let $dv_{in}(t)/dt \approx$

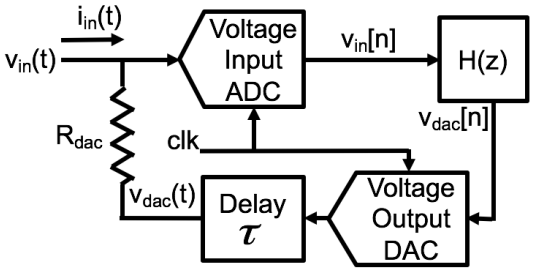

Fig. 1. Block diagram of a clock-tuned Thévenin-form digital discrete-time non-Foster circuit [5]. Digital clock signal clk with frequency $f_c = 1/T_c$ sets the system sample rate. The ADC generates $v_{in}[n] = v_{in}(nT_c)$, which is processed by a digital filter, $H(z)$ with output $v_{dac}[n] = h[n] * v_{in}[n]$, and is converted by the DAC to the continuous-time output voltage $v_{dac}(t)$. DAC source resistance, R_{dac}, sets input current $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$. Latency ,$\tau$, is included to account for processing and conversion time.

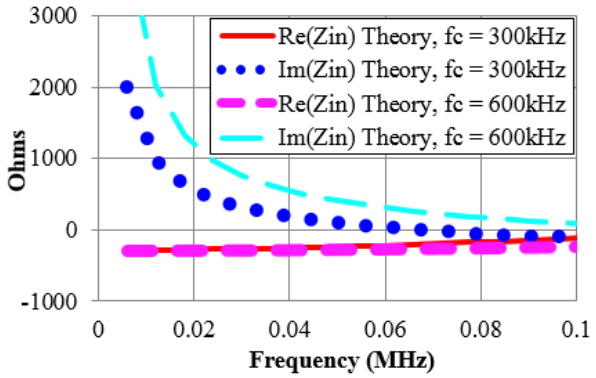

Fig. 2. Theoretical results for clock-tuned digital non-Foster negative capacitance of $C_0 = -5$ nF, with $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and $\tau = T_0 = 1.12\,\mu$s. The solid red curve is $Re(Z_{in}(s, f_c))$ and dotted blue is $Im(Z_{in}(s, f_c))$ at $f_c = 300$ kHz; the short-dashed magenta is $Re(Z_{in}(s, f_c))$, and long-dashed cyan is $Im(Z_{in}(s, f_c))$ at f_c = 600 kHz.

$(v_{in}[n] - v_{in}[n-1])/T_0$ and $i_{in}[n] \approx [v_{in}[n] - v_{dac}[n]]/R_{dac}$ where T_0 is not to be confused with T_c above. Rearranging, $v_{dac}[n]\,(R_{ser}C_0 + T_0) = v_{in}[n]\,(R_{ser}C_0 - R_{dac}C_0 + T_0) + v_{in}[n-1]\,(R_{dac}C_0 - R_{ser}C_0) + v_{dac}[n-1]R_{ser}C_0$.

Taking the z-transform of the foregoing difference equation, and solving for $H(z)$ for the series RC case, yields [6]

$$H_{RC}(z) = \frac{V_{dac}(z)}{V_{in}(z)} = \frac{(R_{ser}C_0 - R_{dac}C_0 + T_0)\,z + (R_{dac}C_0 - R_{ser}C_0)}{(R_{ser}C_0 + T_0)\,z - R_{ser}C_0}. \quad (2)$$

Given $Z_{in}(s, f_c)$ and $H_{RC}(z)$ above, the theoretical relationship between capacitance and variable clock frequency can be derived for the system in Fig. 1. To begin, consider the simple case where latency τ = 0, where $Z_{in}(s, f_c)$ becomes

$$Z_{in}(s, f_c) = \left.\frac{s/f_c\; R_{dac}}{s/f_c - H(z)(1 - z^{-1})}\right|_{z=e^{s/f_c}}. \quad (3)$$

Then, substituting $H_{RC}(z)$ for $H(z)$ and approximating $z = e^{s/f_c} \approx 1 + s/f_c$ for low frequency where $|s/f_c| << 1$, yields

$$Z_{in}(s, f_c) \approx \frac{(R_{ser}C_0 + T_0)\,(1 + s/f_c) - R_{ser}C_0}{sC_0/f_c}. \quad (4)$$

Finally, separating the real and imaginary components gives

$$Z_{in}(s, f_c) \approx \frac{f_c}{sC_0/T_0} + R_{ser} + \frac{T_0}{C_0}, \quad (5)$$

where $R_{ser} + T_0/C_0$ represents a parasitic series resistance. At low frequencies where $|s/f_c| << 1$, the effective capacitance C_e as a function of clock frequency f_c is then

$$C_e(f_c) \approx \frac{C_0}{f_c T_0} = C_0\,\frac{f_0}{f_c}, \quad (6)$$

where f_c is the external clock frequency, C_0 is the design capacitance at frequency $f_0 = 1/T_0$, and $C_e(f_c)$ is the effective capacitance as a function of f_c. Note that $C_e(f_c)$ is inversely proportional to clock frequency f_c.

Fig. 2 shows $Z_{in}(s, f_c)$ from (1) for an $H_{RC}(z)$ example with negative capacitance $C_0 = -5$ nF, $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and $\tau = T_0 = 1.12\ \mu$s. The solid red curve is $Re(Z_{in}(s, f_c))$ and dotted blue is $Im(Z_{in}(s, f_c))$ when f_c = 300 kHz, and the short-dashed magenta is $Re(Z_{in}(s, f_c))$ and long-dashed cyan is $Im(Z_{in}(s, f_c))$ for f_c = 600 kHz. Clearly, capacitance depends on clock frequency f_c, and $Im(Z_{in}(s, f_c))$ has the $|1/sC|$ form of a negative capacitor.

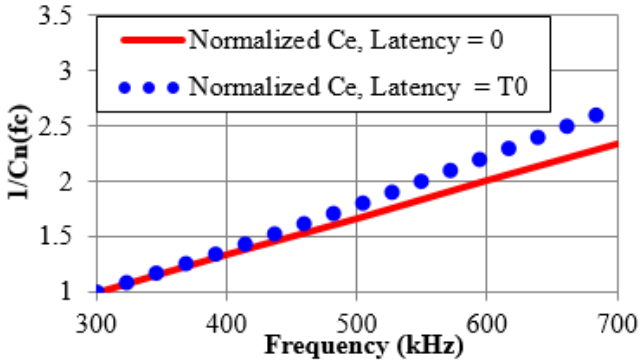

Fig. 3. Inverse of theoretical normalized capacitance $1/C_n(f_c)$ as a function of external clock frequency f_c. The solid red curve is for zero latency, and the dotted blue line is for latency $\tau = T_0$. For both latencies, $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, $C_0 = -5$ nF, T_0 = 1.12 μs, taken at $s = j10^4\pi$.

For analysis purposes, it is also useful to define normalized capacitance $C_n(f_c) = [2\pi \cdot 3 \times 10^5 \cdot Im(Z_{in}(s, 2\pi \cdot 3 \times 10^5)]\ /\ [2\pi f_c Im(Z_{in}(s, 2\pi f_c))]$. This $C_n(f_c)$ represents the capacitance computed from $Im\{Z_{in}(s, f_c)\}$ normalized to the capacitance computed from $Im\{Z_{in}(s, f_c)\}$ at $f_c = 300$ kHz. Fig. 3 shows the inverse of the theoretical normalized capacitance $1/C_n(f_c)$ at 5 kHz as a function of clock frequency f_c for latencies of τ =0 and $\tau = T_0 = 1.12\,\mu$s. From (6), $C_e(f_c)$ at f_c=600 kHz should be half of $C_e(f_c)$ at f_c=300 kHz, and so $1/C_n(f_c)$ should equal 2.0 at 600 kHz, as is observed for the zero-latency case of Fig. 3. For nonzero latency, the simple expression in (6) no longer applies, and capacitance must be calculated from (1). Nevertheless, in Fig. 3, the capacitance for 1.12 μs latency is within ≈20% of the zero latency case.

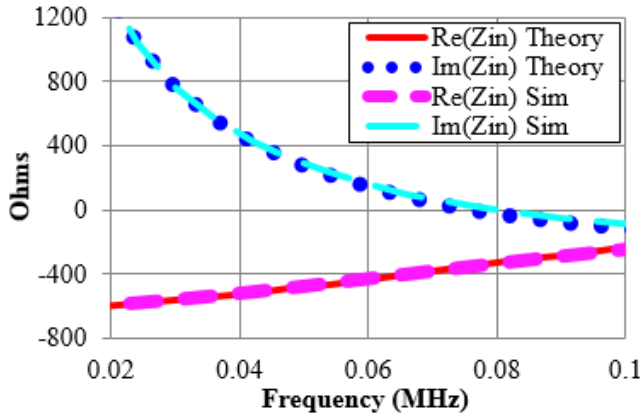

Fig. 4. ADS simulation of a digital non-Foster negative capacitance of $C_0 = -5$ nF. The solid red curve is $Re(Z_{in}(s, f_c))$ and dotted blue is $Im(Z_{in}(s, f_c))$ from (1); the short-dashed magenta and long-dashed cyan curves are the real and imaginary parts of simulated input impedance, where $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, $\tau = T_0 = 1.12\ \mu$s, and f_c = 600 kHz.

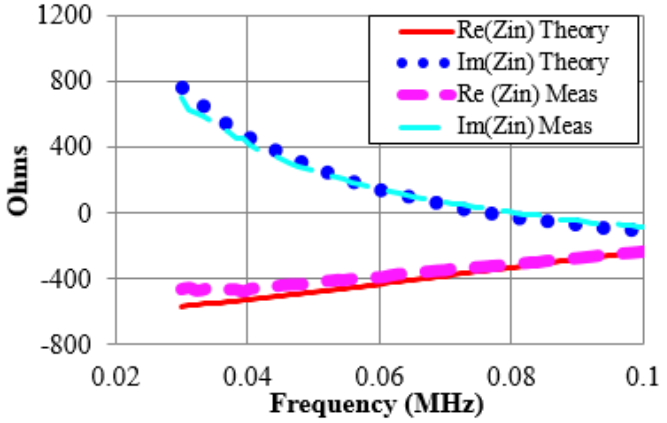

Fig. 5. Measured results for a digital non-Foster negative capacitance of $C_0 = -5$ nF and f_c = 600 kHz. The solid red and dotted blue curves are the real and imaginary parts of theoretical input impedance $Z_{in}(s, f_c)$ from (1). The short-dashed magenta and long-dashed cyan curves are the real and imaginary parts of measured input impedance. Design parameters are $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and $\tau = T_0 = 1.12$ μs.

III. Simulation Results

The system of Fig. 1 was simulated using Keysight ADS large-signal S-parameter simulation. The simulation results in Fig. 4 are compared to the expected theoretical $Z_{in}(s, f_c)$ from (1) for a digital non-Foster negative capacitance of $C_0 = -5$ nF. Remaining design parameters were $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, $\tau = T_0 = 1.12$ μs, and an external clock frequency $f_c = 600$ kHz. In Fig. 4, the solid red and dotted blue curves are the real and imaginary parts of the theoretical input impedance $Z_{in}(s, f_c)$ from (1), and the short-dashed magenta and long-dashed cyan curves are the real and imaginary parts of the simulated input impedance, respectively. The theoretical input impedance at 30 kHz ($s = j60,000\pi$) is $Z_{in}(s, f_c) = -565 + j764$ ohms and compares favorably to the simulated input impedance of $-553 + j765$ ohms. Thus, the simulation results in Fig. 4 are in agreement with theoretical $Z_{in}(s, f_c)$ from (1).

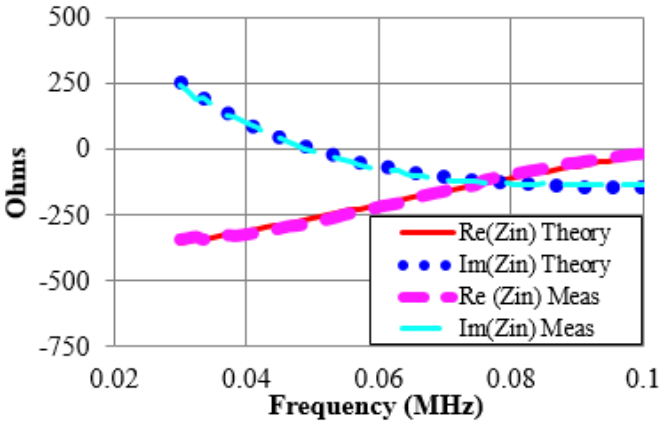

Fig. 6. Measured results for a digital non-Foster negative capacitance of $C_0 = -5$ nF and f_c = 300 kHz. The solid red and dotted blue curves are the real and imaginary parts of theoretical input impedance $Z_{in}(s, f_c)$ from (1). The short-dashed magenta and long-dashed cyan curves are the real and imaginary parts of measured input impedance. Design parameters are $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and $\tau = T_0 = 1.12$ μs.

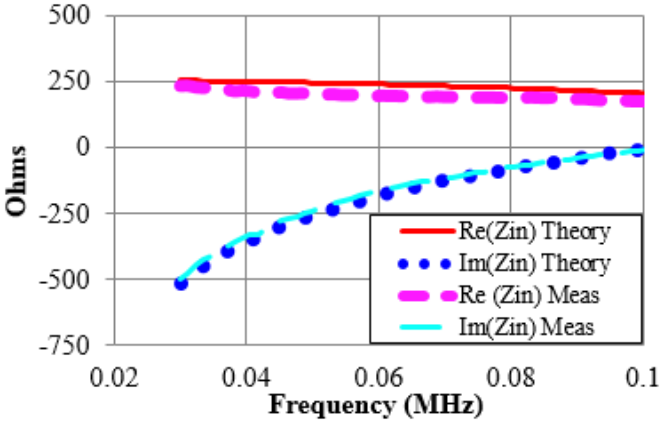

Fig. 7. Measured results for a positive capacitance of $C_0 = 5$ nF and f_c = 600 kHz. The solid red and dotted blue curves are the real and imaginary parts of theoretical input impedance $Z_{in}(s, f_c)$ from (1). The short-dashed magenta and long-dashed cyan curves are the real and imaginary parts of measured input impedance. Design parameters are $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and $\tau = T_0 = 1.12$ μs.

IV. Prototype and Measured Results

A prototype of the system of Fig. 1 was constructed using an NXP FRDM-K64F microcontroller development board with an on-board 16-bit ADC and 12-bit DAC. The signal processing of (2) was programmed onto the board, and the external clock was connected to one of the digital input pins. First, a digital non-Foster negative capacitance was built and tested. Measured results for a clock-tuned digital negative capacitance of $C_0 = -5$ nF are shown in Fig. 5 for f_c = 600 kHz, and shown in Fig. 6 for f_c = 300 kHz. Then, a positive capacitance was built and tested. Similarly, measured results for a clock-tuned positive capacitance $C_0 = 5$ nF are shown in Fig. 7 for f_c = 600 kHz, and Fig. 8 for f_c = 300 kHz.

For the $C_0 = -5$ nF case of Fig. 5 and Fig. 6, the solid red and dotted blue curves show the real and imaginary parts of the theoretical input impedance $Z_{in}(s, f_c)$ from (1), respectively. The short-dashed magenta and long-dashed cyan curves give

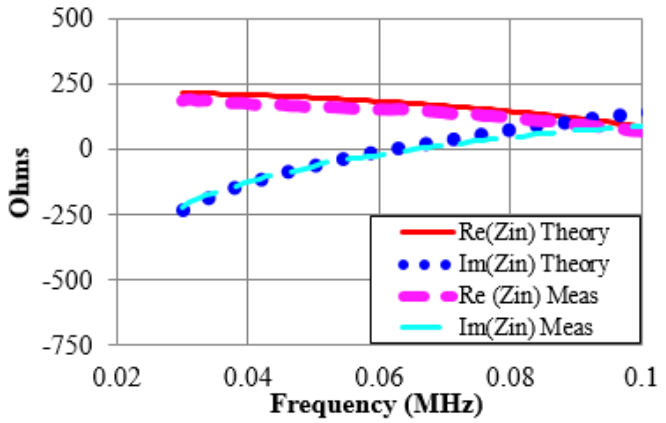

Fig. 8. Measured results for a positive capacitance of $C_0 = 5$ nF and f_c = 300 kHz. The solid red and dotted blue curves are the real and imaginary parts of theoretical input impedance $Z_{in}(s, f_c)$ from (1). The short-dashed magenta and long-dashed cyan curves are the real and imaginary parts of measured input impedance. Design parameters are $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and $\tau = T_0 = 1.12$ μs.

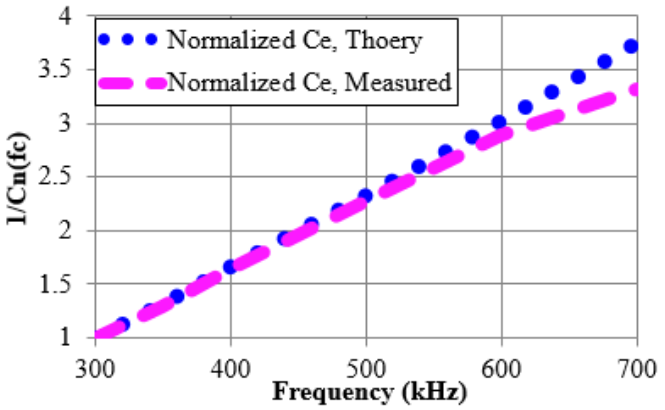

Fig. 9. Measured and theoretical inverse of normalized capacitance $1/C_n(f_c)$ as a function of external clock frequency f_c. The dotted blue curve is the theoretical expectation while the short-dashed magenta line is the measured result. In both cases, $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, $\tau = T_0 = 1.12$ μs, and $C_0 = -5$ nF.

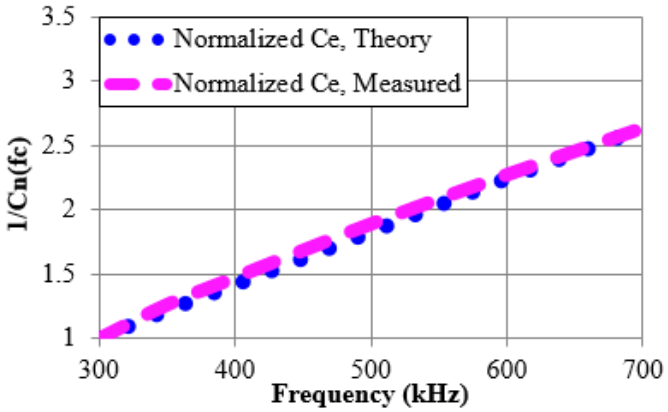

Fig. 10. Measured and theoretical inverse of normalized capacitance $1/C_n(f_c)$ as a function of external clock frequency f_c. The dotted blue curve is the theoretical expectation while the short-dashed magenta line is the measured result. In both cases, $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, $\tau = T_0 = 1.12$ μs, and $C_0 = 5$ nF.

the real and imaginary parts of the measured input impedance. The change in negative capacitance when the clock frequency f_c changes from 600 kHz to 300 kHz is clearly seen by comparing the reactance in Fig. 5 to the reactance in Fig. 6. For both figures, remaining design parameters were $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and latency $\tau = T_0$ = 1.12 μs.

For the negative capacitance in Fig. 5 with f_c = 600 kHz, measured Z_{in} =-459+j704 ohms, corresponding to a capacitance of -7.5 nF, and a quality factor of $|Q|$ = 1.53 at a measurement frequency of 30 kHz ($s = j60,000\pi$). For the negative capacitance in Fig. 6 with f_c = 300 kHz, measured Z_{in} = -341 +j244 ohms, corresponding to a capacitance of -21.8 nF, and $|Q|$ = 0.71 at a measurement frequency of 30 kHz. As noted earlier, non-zero latency can contribute to capacitance changes greater than a factor of two when the clock frequency is reduced by half. Nevertheless, the measured results of Fig. 5 and Fig. 6 are in clear agreement with theoretical predictions from (1).

As noted above, the system of Fig. 1 can also be used to create clock-tuned positive capacitance in addition to negative capacitance. Measured results for clock-tuned positive capacitance are shown in Fig. 7 for f_c = 600 kHz and Fig. 8 for f_c = 300 kHz. For both figures, the solid red and dotted blue curves represent the real and imaginary parts of the theoretical input impedance $Z_{in}(s, f_c)$ from (1), respectively, while the short-dashed magenta and long-dashed cyan curves represent the real and imaginary parts of the measured input impedance. The change in positive capacitance when the clock frequency f_c changes from 600 kHz to 300 kHz is clearly seen by comparing the reactance in Fig. 7 to the reactance in Fig. 8. For both figures, remaining design parameters were $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, and latency $\tau = T_0$ = 1.12 μs.

Fig. 9 shows the measured and theoretical normalized capacitance $C_n(f_c)$ for a negative capacitor of $C_0 = -5$ nF as the external clock was adjusted from f_c=300 kHz to f_c=700 kHz, with the reactance measured at 30 kHz ($s = j60,000\pi$) used to calculate $C_e(f_c)$. At f_c=500 kHz in Fig. 9, measured normalized capacitance was $C_n(5{\times}10^5)$=2.27, while the expected theoretical value was $C_n(5{\times}10^5)$=2.33. Similarly, Fig. 10 shows the measured and theoretical normalized capacitance $C_n(f_c)$ for a positive capacitor of C_0 =5 nF, as the external clock was adjusted from f_c=300 kHz to f_c=700 kHz, with the reactance measured at 30 kHz used to calculate $C_e(f_c)$. At f_c = 500 kHz in Fig. 10, measured normalized $C_n(5{\times}10^5)$=1.89, while the theoretical expectation was $C_n(5{\times}10^5)$=1.83. For both Fig. 9 and Fig. 10, the remaining design parameters were $R_{ser} = 1$ ohm, $R_{dac} = 1000$ ohms, $\tau = T_0 = 1.12$ μs.

As noted earlier, the prototype of the system of Fig. 1 is implemented using a FRDM-K64F development board, as shown in Fig. 11. A digital input pin of the microcontroller is used to receive the external clock signal of Fig. 1, setting the sample rates of the on-board 16-bit ADC and 12-bit DAC.

V. Conclusion

A clock-tuned digital non-Foster circuit is described, including theory, simulation results, and measurements of a prototype constructed using a FRDM-K64F development board. Measurements confirm clock-tunable positive and negative capacitance in line with theory, even in the presence of non-zero latency. Simulations and measurements of the prototype are in close agreement with theory, confirming the overall efficacy of the underlying theory and proposed approach.

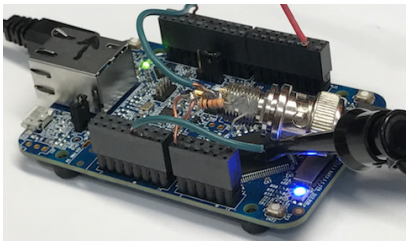

Fig. 11. Prototype using FRDM-K64F development board.

REFERENCES

[1] D. Gregoire, C. White, and J. Colburn, "Wideband artificial magnetic conductors loaded with non–Foster negative inductors," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1586–1589, 2011.

[2] S. Hrabar, I. Krois, I. Bonic, and A. Kiricenko, "Negative capacitor paves the way to ultra-broadband metamaterials," *Applied Physics Letters*, vol. 99, no. 25, p. 254103, 2011.

[3] C. Robey, Frank, M. Hancock, Timothy, and B. Stahl, Gregory, "Digital matching of a radio frequency antenna," published on WIPO patentscope.wipo.int as WO2016028354 on Feb. 25, 2016, International Patent Application No. PCT/US2015/033742 filed Jun. 2, 2015.

[4] N. Zhu and R. W. Ziolkowski, "Active metamaterial-inspired broadbandwidth, efficient, electrically small antennas," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1582–1585, 2011.

[5] T. P. Weldon, J. M. C. Covington, K. Smith, and R. S. Adams, "Performance of digital discrete-time implementations of non-Foster circuit elements," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2169–2172.

[6] P. J. Kehoe, K. K. Steer, and T. P. Weldon, "Thevenin forms of digital discrete-time non-Foster RC and RL circuits," in *2016 IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Jun. 2016, pp. 191–192.

[7] K. K. Steer, P. J. Kehoe, and T. P. Weldon, "Effects of latency and quantization noise on digital discrete-time non-Foster circuits," in *2016 IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Jun. 2016, pp. 731–732.

[8] T. P. Weldon, "Digital discrete-time non-Foster circuit elements and non-Foster circuits with optional adaptive control means," US Patent Pending 61/061,441, Oct. 8, 2014.

[9] C. Phillips and H. Nagle, *Digital Control System Analysis and Design*. Prentice-Hall, 1990.