Investigation of an Adaptively-Tuned Digital Non-Foster Approach for Impedance Matching of Electrically-Small Antennas

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***Abstract*—An adaptively-tuned digital non-Foster negative capacitor is investigated for impedance matching of electrically-small antennas. Such a digital non-Foster approach has the potential to address difficult design challenges such as stability and tolerance issues in analog non-Foster circuits. Furthermore, the digital non-Foster approach is tunable in software. The required negative capacitance is implemented using an ADC (analog-to-digital converter), DAC (digital-to-analog converter), and signal processing. In addition, the proposed adaptive approach uses the DAC and ADC to excite the antenna with a signal, and determine the antenna capacitance and resistance using impulse response and/or ARMA modeling. The digital non-Foster negative capacitance is then used to cancel the observed undesired reactance of the antenna. Results are given for an RC model of an electrically-short antenna that show effective estimation of impedance, and successful cancellation of most of the undesired reactance.**

I. Introduction

A serious impediment to the design of mobile electrically-small antennas much below 800 MHz is the fundamental Wheeler-Chu limit that results in a collapse in bandwidth proportional to the cube of antenna dimensions [1]–[3]. As validated with over 50 years (through 2010) of published antenna data, the bandwidth of a small antenna decreases by a factor of more than 1000 as size decreases by a factor of 10 [4]. However, recent results show that Wheeler-Chu small-antenna bandwidth limits can be overcome by using non-Foster methods to significantly enhance the performance and bandwidth of electrically-small antennas [5]–[9]. Thus, the proposed digital non-Foster approach has potential for software-reconfigurable, wideband, and adaptive enhancements of small antennas over broad swaths of spectrum as needed in wideband software defined radio [10]–[16]. Such non-Foster circuits have also found important applications in acoustics [17]. Importantly, the architecture of the digital non-Foster approach has the potential to be readily integrated/adapted in SDRs (software-defined radios), where the required ADC (analog-to-digital converter) could be implemented in the receiver, and the required DAC (digital-to-analog converter) implemented in the transmitter [11], [12].

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Prior adaptively tuned non-Foster circuits have been limited to analog implementations [18], [19]. In contrast the proposed approach is a digital implementation. A digital non-Foster approach lends itself to dynamic adaptive tuning and stabilization that can adjust to antenna impedance variations due to movement and nearby objects. Such practical variations can also affect stability issues that remain significant design concern in analog non-Foster approaches [20], [21].

In the following section, theory for a digital non-Foster RC (resistor-capacitor) circuit is presented. Next, two adaptive approaches are presented. Simulation results are then presented for adaptive estimation of antenna impedance. In Section 5, simulation results are presented showing the effective cancellation of undesired antenna reactance.

II. Digital non-Foster Antenna Matching

In this section, background theory is presented for antenna impedance matching using a digital discrete-time non-Foster as in Fig. 1. Other approaches are possible, but the example of Fig. 1 suffices to illustrate the principles. Fig. 1 includes a Thévenin RC model of an electrically-small antenna on the left, and a digital non-Foster circuit for impedance matching on the right. Following the digital non-Foster design in [22], the ADC in Fig. 1 with clock period T digitizes continuous-

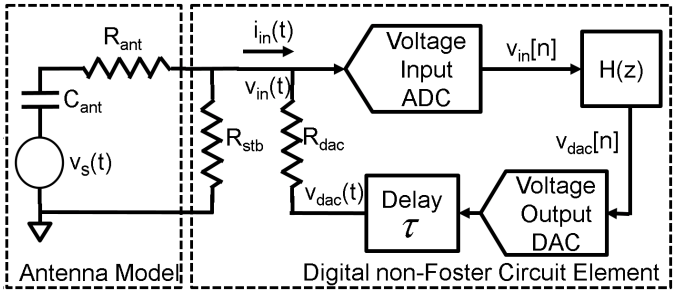

Fig. 1. Block diagram of an RC model for an electrically-small antenna with a digital non-Foster matching circuit. ADC with clock period T yields $v_{in}[n] = v_{in}(nT)$, discrete-time filter $H(z)$ outputs $v_{dac}[n] = h[n] * v_{in}[n]$, with $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$, where time latency τ is included, and R_{stb} is added to improve overall circuit stability.

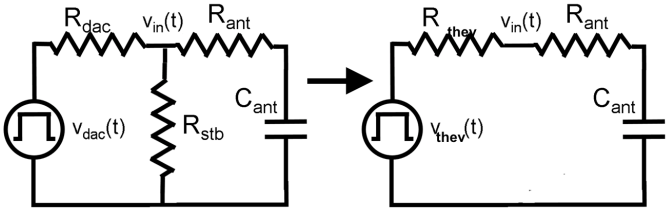

Fig. 2. Circuit schematic for block diagram of Fig. 1 with signal processing block $H(z) = 0$ and pulse excitation $v_{dac}[n] = \delta[n]$ applied to the DAC, with Thévenin equivalent circuit for analysis shown at right.

time input voltage $v_{in}(t)$, generating discrete-time voltage $v_{in}[n] = v_{in}(nT)$. Signal processing is performed by $H(z)$ to form the DAC signal $v_{dac}[n] = h[n] * v_{in}[n]$, where $H(z)$ is the z-transform of $h[n]$. The current through R_{dac} is then $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$, where provision is also added to account for latency τ associated with computation time and conversion time. Taking the Laplace transform of $v_{dac}(t)$ gives $V_{dac}(s) = V^{\star}(s)H(z)(1 - z^{-1})e^{-s\tau}/s\big|_{z=e^{sT}}$, assuming a zero-order hold, and where $V^{\star}(s) = \sum v(nT)e^{-nsT}$ is the starred transform [23]. The impedance looking into the right of v_{in} is then [22]

$$Z(s) \approx \frac{sT\, R_{dac}}{sT - H(z)(1 - z^{-1})e^{-s\tau}}\bigg|_{z=e^{sT}} \tag{1}$$

for $v_{in}(t)$ sampled without aliasing and frequencies below $0.5/T$ Hz. The total impedance seen by the antenna, including the resistance R_{stb} of Fig. 1 is then the parallel combination

$$Z_{tot}(s) = Z(s)||R_{stb}\ , \tag{2}$$

which is used to match the antenna impedance.

Next, consider the antenna model on the left of Fig. 1. Ideally, the matching network would cancel the typically large reactance of C_{ant} for an electrically-small antenna, but may also transform the real part of the impedance R_{ant}. The total impedance at $v_s(t)$ looking into the antenna in series with the non-Foster element is

$$Z_{in}(s) = Z_{tot}(s) + R_{ant} + \frac{1}{sC_{ant}}\ , \tag{3}$$

where the negative capacitance of the digital non-Foster circuit ideally cancels the positive capacitance C_{ant} of the antenna (here assuming an electrically-small monopole). It is also important to note that in SDR applications, $v_{in}[n]$ at the output of the ADC may also be used as the radio input signal of an SDR [11], [12].

III. Adaptive non-Foster Tuning Approaches

The adaptive non-Foster tuning of the antenna impedance is now considered, given the foregoing result for the total impedance. As one approach, the DAC of Fig. 1 can be used as an independent signal source (impulse, psuedo-random, etc.) to measure the impedance of the antenna from observed ADC voltages. As a simple example, signal processing block $H(z)$ can be disabled ($H(z) = 0$), and a digital pulse $v_{dac}[n] = \delta[n]$ can be applied to the DAC. The equivalent circuit is shown in

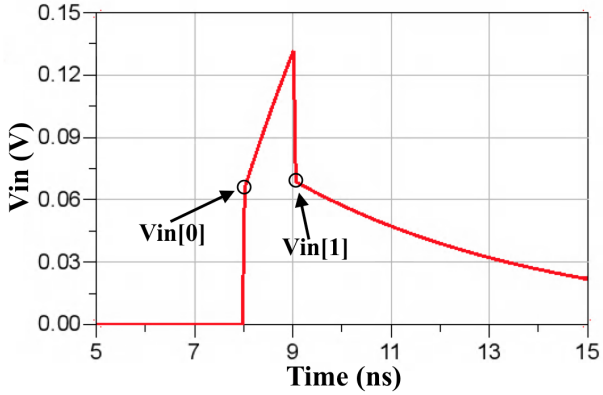

Fig. 3. ADS time-domain simulation results for $v_{in}(t)$ of Fig. 1 with $H(z) = 0$ and 1-volt DAC pulse excitation $v_{dac}[n] = \delta[n]$. $v_{in}[0]$ is the ADC voltage when the capacitor is initially discharged, and $v_{in}[1]$ is the ADC voltage just after the DAC pulse when the capacitor begins to discharge.

Fig. 2, and time-domain simulation of $v_{in}(t)$ for 1-volt DAC pulse is shown in Fig. 3.

For analysis purposes, the left of Fig. 2 was converted to Thévenin-form with $R_{thev} = (R_{dac}R_{stb})\,/\,(R_{dac} + R_{stb})$, and pulse voltage $v_{thev}[n] = (v_{dac}[n]R_{stb})\,/\,(R_{dac} + R_{stb})$. After this conversion, the circuit becomes a simple series RC network on the right of Fig. 2, with series capacitance C_{ant}, and total series resistance $R_{thev} + R_{ant}$. R_{dac} and R_{stb} are part of the non-Foster circuit element, and therefore are either known or can be set to a desired value. Thus, from the right of Fig. 2, when the capacitor is initially discharged with no voltage, the initial ADC voltage $v_{in}[0] = v_{in}(0)$ is

$$v_{in}[0] \approx \frac{R_{ant}v_{thev}[0]}{R_{ant} + R_{thev}} = \frac{R_{ant}}{R_{ant} + R_{thev}}\frac{R_{stb}}{R_{dac} + R_{stb}}, \tag{4}$$

where $v_{dac}(t)$ is a 1-volt pulse of width T, and $v_{in}[0]$ the voltage seen at the input of the ADC at the beginning of the input pulse. After rearranging, R_{ant} can be found as

$$R_{ant} = \frac{v_{in}[0]}{v_{thev}[0] - v_{in}[0]}R_{thev}\ . \tag{5}$$

Immediately after the 1-volt DAC pulse $v_{dac}(t)$ of width T, $v_{thev}[1] = 0$, and the capacitor has been fully charged to a voltage $v_c[1]$ on the right of Fig. 2. The voltage $v_c[1]$ arises from the charge on C_{ant}, and for small T may be approximated from the average of initial and final values of the current during the DAC pulse. The initial current is $i_{init} = v_{thev}[0]/(R_{ant}+R_{thev})$, when the capacitor is initially discharged with no voltage. The current just before the end of the pulse is $i_{end} = (v_{thev[0]} - v_c[1])/(R_{thev}+R_{ant})$, when the capacitor has been fully charged to voltage $v_c[1]$ on the right of Fig. 2. Thus, the capacitor voltage at the end of the pulse is $v_c[1] = q/C_{ant} \approx T(i_{init} + i_{end})/(2C_{ant})$. After the DAC pulse, $v_{thev}[1] = 0$, and $v_{in}[1] = v_c[1]R_{thev}/(R_{thev} + R_{ant})$. Substituting for $v_c[1]$ and rearranging yields the ADC voltage just after the 1 volt DAC pulse as

$$v_{in}[1] = \frac{2R_{thev}v_{thev}[0]}{R_{thev} + R_{ant}}\ \frac{1}{1 + 2\,(R_{thev} + R_{ant})\,\frac{C_{ant}}{T}}\ , \tag{6}$$

and solving for C_{ant} yields

$$C_{ant} = \frac{(2v_{thev}[0]R_{thev}-(R_{thev}+R_{ant})v_{in}[1])T}{2v_{in}[1](R_{thev}+R_{ant})^2} . \quad (7)$$

The two equations for R_{ant} and C_{ant} can then be used to solve for the antenna resistance and capacitance for a 1-volt DAC pulse using relations (5) and (7), the measured ADC voltages $v_{in}[0]$ and $v_{in}[1]$, and the known values of $v_{thev}[0]$, R_{thev} and T. *And so, the first adaptive non-Foster antenna tuning approach uses the antenna capacitance estimate from (7) to determine tuning.*

The second adaptive non-Foster antenna tuning approach uses an ARMA model which may better handle the more general case where the excitation is not an impulse. To derive the ideal ARMA model, consider a 1-volt DAC pulse is applied, and the capacitor on the right side of Fig. 2 discharges from initial voltage $v_c[1]$ with time constant $(R_{ant} + R_{thev})C_{ant}$. From the foregoing analysis in (4) and (6), and the time constant after the impulse, the discrete-time impulse response is

$$v_{in}[n] = v_{in}[0]\delta[n] + v_{in}[1]\alpha^{n-1}u[n-1] \quad (8)$$

where

$$\alpha = e^{-T/[(R_{ant}+R_{thev})C_{ant}]} . \quad (9)$$

Finally, taking the z-transform yields the ideal ARMA model for observed ADC voltage $v_{in}[n]$

$$\begin{aligned} V_{in}(z) &= v_{in}[0] + \frac{v_{in}[1]}{z-\alpha} \quad (10) \\ &= \frac{v_{in}[0]z - \alpha v_{in}[0] + v_{in}[1]}{z-\alpha} . \end{aligned}$$

Thus, the second adaptive non-Foster antenna tuning approach, uses the ARMA model of (10) to estimate $v_{in}[0]$, $v_{in}[1]$, and α in (10). As in the first approach, the two equations for R_{ant} in (5) and C_{ant} in (7) along with the known values of $v_{thev}[0]$, R_{thev}, and T can then be used to solve for the antenna resistance and capacitance.

IV. Adaptive Impedance Estimation Results

The proposed adaptive non-Foster tuning is based on adaptively estimating antenna impedance. The ADS time-domain simulation of Fig. 3 was used to evaluate the ability to adaptively estimate the antenna impedance using a DAC pulse and ADC voltages with $H(z) = 0$. The voltage at the ADC input $v_{in}(t)$ is displayed in Fig. 3 for R_{ant} = 15 ohms and C_{ant} = 50 pF, when excited by a 1 V DAC pulse of width T = 1 ns, with $H(z) = 0$.

In the first approach to adaptive impedance estimation, R_{ant} is estimated using (5) and the measured voltage $v_{in}[0]$ of Fig. 3 as well as known values of $v_{thev}[0]$ and R_{thev}. For the measured $v_{in}[0] = 0.064$ volts from Fig. 3, the calculated resistance of the external antenna is $R_{ant} = 14.9$ ohms. Similarly, it is possible to estimate C_{ant} from (7) using measured $v_{in}[0]$ and $v_{in}[1]$ and known values of R_{thev} and T. For the measured of $v_{in}[0] = 0.064$ volts and $v_{in}[1] = 0.069$ volts

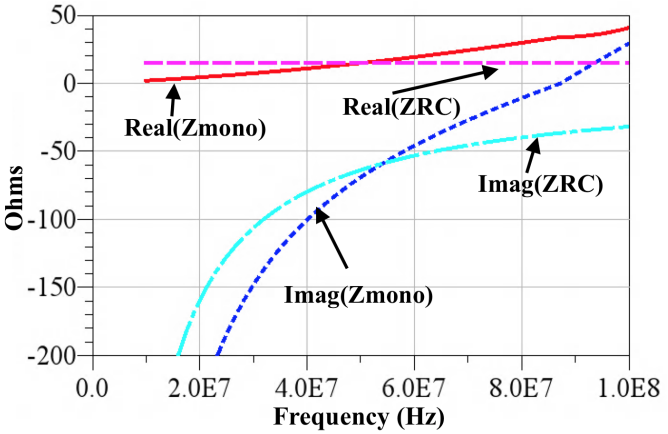

Fig. 4. ADS simulation results comparing input impedance of the RC antenna model, $Z_{RC}(s) = R_{ant} + 1/(sC_{ant})$ to the input impedance Z_{mono} of a 0.75 m long monopole antenna. The solid red and dotted blue lines are $Re(Z_{mono})$ and $Im(Z_{mono})$, the short-dash magenta and long-dash cyan lines are $Re(Z_{RC})$ and $Im(Z_{RC})$.

from Fig. 3 the calculated capacitance of the external antenna is $C_{ant} = 48$ pF.

The second approach to adaptive impedance estimation uses the ARMA method. The antenna impedance is evaluated by using the ARMA model in (8) and experimental data to determine the ARMA parameters. Ideally, the theoretical ARMA parameters in (10) for the antenna model of Fig. 1 with $R_{ant} = 15$ ohms and $C_{ant} = 50$ pF are

$$V_{inTheory}(z) = \frac{0.064z + 0.0119}{z - 0.825} \quad (11)$$

where (4) gives $v_{in}[0]$, (6) gives $v_{in}[1]$, and (9) gives α. Next, using the first 16 points of the observed simulation values of $v_{in}[n]$ from Fig. 3, the MATLAB "armax" function yields the extracted ARMA model

$$V_{inExtract}(z) = \frac{0.069z + 0.012}{z - 0.825}, \quad (12)$$

which compares very favorably with the theoretical value $V_{inTheory}[z]$ in (11). From (12), the values of $C_{ant} = 47.1$ pF and $R_{ant} = 16.3$ ohms are computed using (10), (5), and (7). Note also that the ARMA method can be more generally used to extract the antenna model for input excitation other than a pulse, such as white noise or other waveforms.

V. Impedance Match Simulation

Simulations were performed in Keysight ADS to demonstrate stable impedance matching using a non-Foster circuit element in series with an RC model of an electrically-short monopole antenna. As illustrated in Fig. 1, the antenna is modeled by the series combination of R_{ant} = 15 ohms and C_{ant} = 50 pF. Impedance matching was accomplished with the connection of the digital non-Foster RC circuit element in Fig. 1, with a target design capacitance, C = -47.1 pF and series resistance, R_{ser} = -5 ohms. The -47.1 pF value was obtained using the adaptive ARMA estimate, as described in

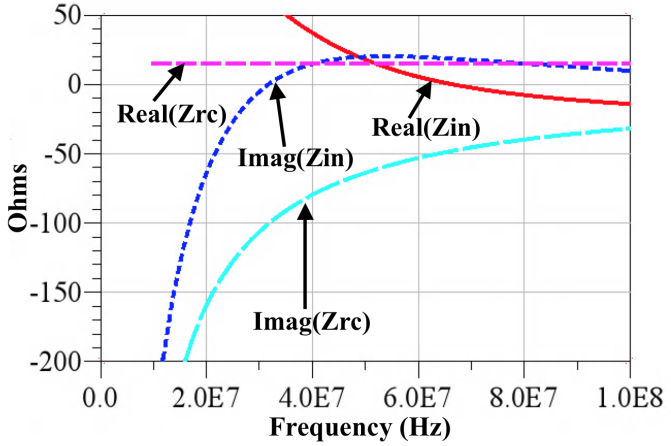

Fig. 5. ADS large-signal S-parameter simulation results comparing input impedance of the RC antenna model, $Z_{RC}(s) = R_{ant} + 1/(sC_{ant})$ to the input impedance of the system $Z_{in}(s)$ after incorporating the digital non-Foster circuit element of Fig. 1. The solid red and dotted blue lines are $Re(Z_{in}(s))$ and $Im(Z_{in}(s))$, the short-dash magenta and long-dash cyan lines are $Re(Z_{RC})$ and $Im(Z_{RC})$.

the previous section. Other parameters were R_{dac}=200 ohms, R_{stb}=160 ohms, T = 1 ns, and τ = 0 ns.

Fig. 4 compares the unmatched RC antenna model using R_{ant} = 15 ohms, C_{ant} = 50 pf, with the target application of a 0.75 m long monopole antenna impedance over the frequency band of interest. At the target design frequency of 50 MHz, the monopole has a reactance of $15 - j68$ ohms, and a moderate Q of 4.5. As seen in Fig. 4, the RC model gives a good approximation between 40 and 60 MHz, and fair approximation from 20 to 80 MHz.

Fig. 5 compares the input impedance of the RC antenna model, $Z_{RC}(s) = R_{ant} + 1/(sC_{ant})$, to the simulated input impedance $Z_{in}(s)$ of (3) of the overall system after incorporating the digital non-Foster matching circuit of Fig. 1. The solid red and dotted blue lines, respectively, represent the real and imaginary parts of the digital non-Foster matched input impedance $Z_{in}(s)$. The short-dash magenta and the long-dash

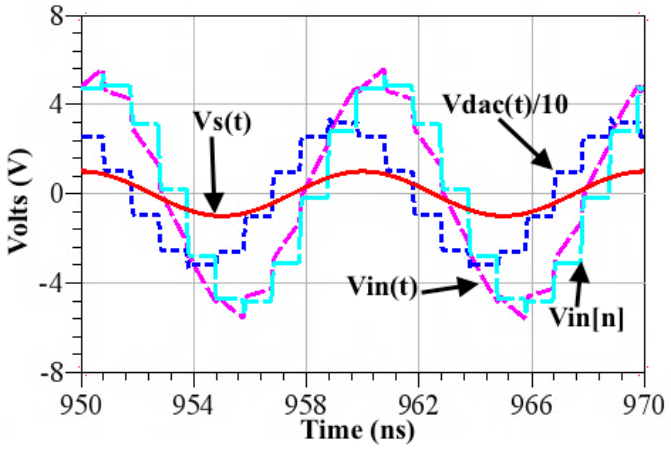

Fig. 6. ADS time-domain simulation results system for Fig. 1 where V_{in} is the voltage seen at the input terminals of the antenna. Here R_{ant} = 15 ohms, C_{ant} = 50 pf, R_{ser} = -5 ohms, T = 1 ns, τ = 0 ns, and the target design capacitance C = -50 pf.

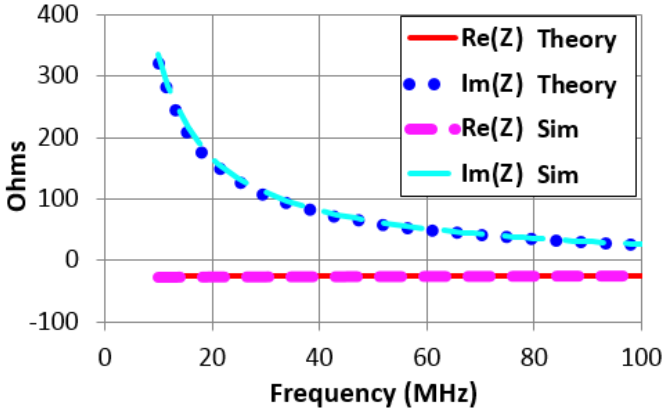

Fig. 7. ADS large signal S-parameter simulation showing impedance $Z(s)$ of digital the non-Foster circuit without R_{stb}, with a target design capacitance, C = -50 pF and series resistance, R_{ser} = -5 ohms, T = 1 ns, τ = 0 ns. The solid red and solid blue curves are the real and imaginary parts of theoretical $Z(s)$ from (1), and dashed magenta and dotted cyan are ADS simulation results.

cyan lines, respectively, represent the real and imaginary parts of the antenna model impedance $Z_{RC}(s)$. At 50 MHz, $Z_{RC}(s)$ was $15 - j63$ ohms, and the digital non-Foster matched antenna impedance of Fig. 1 was reduced to $17.2 + j20.2$ ohms. The magnitude of the antenna reactance was reduced by 68%. Strictly speaking, reducing the reactance is not impedance matching, however canceling antenna reactance and reducing Q from 4.2 to 1.2 suffices for present purposes.

Fig. 6 shows the corresponding time-domain simulation, verifying stable operation, and showing the analog input source $v_s(t)$, non-Foster input $v_{in}(t)$, and digitized waveforms corresponding to $v_{in}[n]$ and $v_{dac}(t)/10$. Lastly, Fig. 7 shows large-signal S-parameter simulation and theoretical impedance of the digital non-Foster circuit, with a target design capacitance, C = -50 pF and series resistance, R_{ser} = -5 ohms, T = 1 ns, τ = 0 ns.

VI. Conclusion

Approaches to adaptive impedance matching of an antenna using digital non-Foster circuits have been presented. Results show effective reduction of the undesired reactance of an electrically-short antenna. Effective estimation of antenna impedance is also demonstrated using ARMA and impulse response methods.

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