# Stability Analysis and Measurement of RC and RL Digital Non-Foster Circuits with Latency

Patrick J. Kehoe, Killian K. Steer, and Thomas P. Weldon
Department of Electrical and Computer Engineering
University of North Carolina at Charlotte
Charlotte, NC, USA
tpweldon@uncc.edu

***Abstract*—Stability analysis and measurements are presented for negative capacitance and negative inductance designs of digital non-Foster circuits that include a series resistance and model the effects of latency. Such digital non-Foster circuits provide a new important alternative to analog non-Foster circuits, with potential to address stability and performance issues in important non-Foster application areas such as metamaterials, acoustic cloaking, and electrically-small antennas. The proposed approach includes a resistive component in the signal processing of digital non-Foster RC and RL circuits to help control stability and to mitigate parasitic resistance, and also includes latency effects associated with computation and conversion time. Analysis, simulation, and measured results confirm the desired non-Foster impedances, and show useful regions of stability as a function of resistance and latency.**

## I. Introduction

Non-Foster circuits such as negative capacitors and negative inductors are of importance in enabling a number of exotic emerging technologies such as acoustic invisibility [1], [2], superluminal waveguides [3], [4], software-designed radios and electrically-small antennas beyond the Wheeler-Chu limit [5]–[8], and metamaterials [9], [10]. Notwithstanding so many promising applications, stability remains a central design issue with non-Foster circuits [11], [12]. More recently, digital non-Foster circuits have been proposed, with the potential of leveraging inherent advantages of digital technology to design repeatably stable digital implementations of non-Foster circuits [13], [14].

The following extends prior stability results in [15] to new Thévenin-form digital non-Foster RC (resistor-capacitor) and RL (resistor-inductor) circuits in [16] that have a voltage-output DAC (digital-to-analog converter), and that include the effects of latency associated with computation time and DAC and ADC (analog-to-digital converter) conversion times. Prior digital non-Foster stability analyses were limited to Norton-form implementations with a current-output DAC, and did not include effects of series resistance and latency [15]. The new stability analysis also considers a series resistance that is included within the signal processing of the digital non-Foster circuit, to provide additional control of stability, and to mitigate parasitic resistance. Therefore, root locus analyses for these new digital non-Foster configurations are presented below, to determine stable regions of operation.

978–1–5386–1539–3/17/$31.00 © 2017 IEEE

In the following section, background theory is reviewed for Thévenin-form digital discrete-time non-Foster RC and RL circuits. In Section III, stability theory is presented and root locus analysis is used to determine stable regions of operation. Lastly, measured results are provided for several stable prototype circuits and compared against theoretical results.

## II. Digital non-Foster RC and RL Theory

Before proceeding with root locus stability analysis in the following section, the theory of Thévenin-form digital discrete-time non-Foster circuits is reviewed [16]. In Fig. 1, a Thévenin-form digital non-Foster circuit is driven by an external Norton current source. Non-Foster input voltage $v_{in}(t)$ is converted into discrete time signal $v_{in}[n] = v_{in}(nT)$ by the ADC with clock period $T$. Signal processing block $H(z)$ produces the voltage-output DAC signal $v_{dac}[n] = h[n] * v_{in}[n]$. The final DAC output $v_{dac}(t)$ typically includes a ZOH (zero-order hold) and latency effects (associated with computation time and DAC and ADC conversion times) modeled as time delay $\tau$. Also, the DAC has a finite source resistance (and/or added external resistance), which is represented by $R_{dac}$. From $R_{dac}$, the input current is $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$. The Laplace transform, assuming a ZOH, gives $V_{dac}(s) = V_{in}^{\star}(s)H(z)(1-z^{-1})e^{-s\tau}/s\big|_{z=e^{sT}}$ where

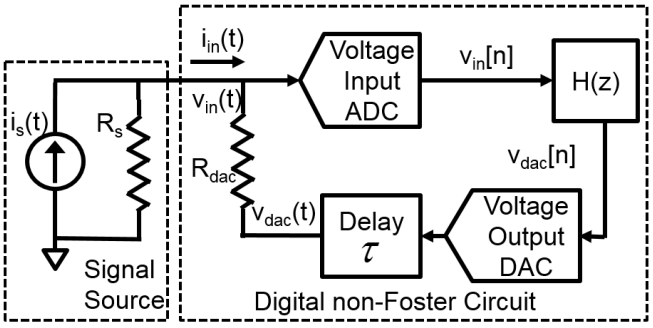


Fig. 1. Block diagram of a Thévenin-form digital discrete-time non-Foster circuit [13] driven by external Norton current source $i_s(t)$ [15]. ADC with clock period $T$ converts input voltage into $v_{in}[n] = v_{in}(nT)$, with filter $H(z)$ output $v_{dac}[n] = h[n] * v_{in}[n]$, DAC output voltage $v_{dac}(t)$, latency $\tau$, and current $i_{in}(t) = [v_{in}(t) - v_{dac}(t)]/R_{dac}$.

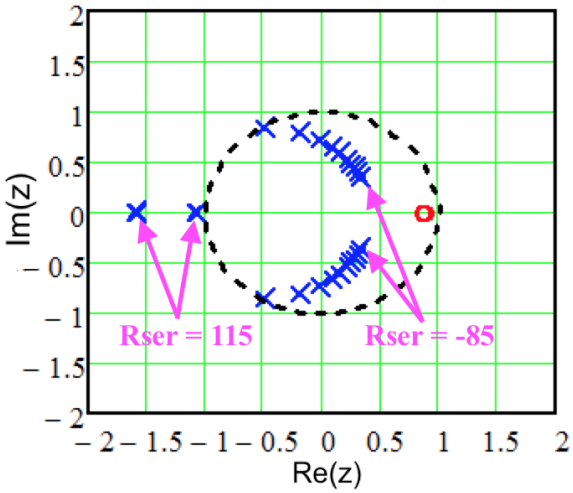


Fig. 2. Root locus stability analysis of $G(z)$ for a digital non-Foster RC circuit element with C = $-8$ nF, and $R_{ser}$ varied from $-85$ ohms to 115 ohms in steps of 20. The edge of stability occurs near $R_{ser} \approx 100$ ohms. Other parameters were $R_s = 50$ ohms, $R_{dac}$ = 1000 ohms, $\lambda = 1$, and $T = 1120$ ns. Poles are denoted "X," and zeroes denoted "O."

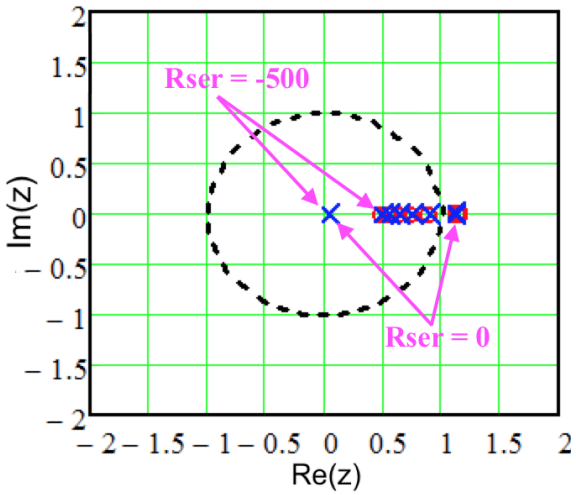


Fig. 3. Root locus stability analysis of $G(z)$ for a digital non-Foster RL circuit element with L = $-0.5$ mH, and $R_{ser}$ varied from $-500$ ohms to 0 ohms in steps of 100. The edge of stability occurs near $R_{ser} \approx -50$ ohms. Other parameters were $R_s = 50$ ohms, $R_{dac}$ = 1000 ohms, $\lambda = 1$, and $T = 1260$ ns. Poles are denoted "X," and zeroes denoted "O."

$V^\star(s) = \sum v(nT)e^{-nsT}$ is the the starred transform [17]. For $v_{in}(t)$ sampled at $0.5/T$ Hz without aliasing, the impedance of the digital non-Foster circuit element in the dashed box on the right side of Fig. 1 is [16]

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \left.\frac{sT\ R_{dac}}{sT - H(z)(1-z^{-1})e^{-s\tau}}\right|_{z=e^{sT}}. \quad (1)$$

The circuit of Fig. 1 and (1) can be used to design a range of digital implementations of non-Foster circuits, such as negative capacitors, negative inductors, and the non-Foster RC and RL circuits in [16].

For present purposes, first consider an analog series RC circuit with capacitance C and resistance $R_{ser}$. For this circuit, $v(t) = i(t)R_{ser} + \int i(t)dt/C$. Next, taking the derivative gives $dv_{in}(t)/dt = R_{ser}di_{in}(t)/dt + i_{in}(t)/C$. Approximating, $dv_{in}(t)/dt \approx (v_{in}[n] - v_{in}[n-1])/T$ and $i_{in}[n] \approx (v_{in}[n] - v_{dac}[n])/R_{dac}$, the circuit can be realized as $v_{dac}[n]\ (R_{ser}C + T) = v_{in}[n]\,(R_{ser}C - R_{dac}C + T) + v_{in}[n-1]\,(R_{dac}C - R_{ser}C) + v_{dac}[n-1]R_{ser}C$. Taking the z-transform yields $H(z)$ for the digital series RC [16]

$$H_{RC}(z) = \frac{(R_{ser}C - R_{dac}C + T)\,z + (R_{dac}C - R_{ser}C)}{(R_{ser}C + T)\,z - R_{ser}C}. \quad (2)$$

The same approach can be applied to an analog series RL circuit with inductance L and resistance $R_{ser}$. For this circuit, $v(t) = Ldi(t)/dt + i(t)R_{ser}$. Approximating $di_{in}(t)/dt \approx (i_{in}[n] - i_{in}[n-1])/T$ and with $i_{in}[n] \approx (v_{in}[n] - v_{dac}[n])/R_{dac}$ , the equation can be realized as $v_{dac}[n]\,(1 + R_{ser}T/L) - v_{dac}[n-1] = v_{in}[n](1 + R_{ser}T/L - R_{dac}T/L) - v_{in}[n-1]$. Taking the z-transform yields [16]

$$H_{RL}(z) = \frac{(L + R_{ser}T - R_{dac}T)\,z - L}{(L + R_{ser}T)\,z - L} \quad (3)$$

## III. Stability Analysis

When the non-Foster RC element is connected to the Norton source, as seen in Fig. 1, the closed-loop system transfer function relating the source current to the non-Foster input current (DAC current) is $G(s) = I_{in}(s)/I_s(s)$ with corresponding discrete-time transfer function [15], [17]

$$G(z) = \frac{-R_e z^{-\lambda} H(z)/R_{dac}}{1 - R_e z^{-\lambda} H(z)/R_{dac}}, \quad (4)$$

where $\lambda$ is the (integer) latency in clock cycles, $R_e = R_s R_{dac}/(R_s + R_{dac})$ is the parallel combination of the source and DAC resistances, and $V_{in}(z)H(z)z^{-\lambda}/R_{dac}$ would be the Norton-equivalent current of the Thévenin source comprised of the voltage-output DAC in series with $R_{dac}$. Then, the system of Fig. 1 is stable as long as the poles of $G(z)$ in (4) lie within the unit circle [17].

Root locus analysis was performed on (4) to investigate the range of stable values of $R_{ser}$. The example of Fig. 2 shows the root locus plot for a digital non-Foster RC design of a $C = -8$ nF capacitor, as $R_{ser}$ was increased from $-85$ ohms to 115 ohms in steps of 20. Other parameters for $H(z) = H_{RC}(z)$ in Fig. 2 were $T = 1120$ ns, $R_{dac} = 1000$ ohms, $\lambda = 1$, and $R_s = 50$ ohms. At $R_{ser} = -85$ ohms, the two poles of $G(z)$ are well within the unit circle. The poles become unstable and move outside the unit circle at $R_{ser} = 115$ in Fig. 2. The stability boundary was observed near $R_{ser} \approx 100$ ohms, with instability for $R_{ser} > 100$ ohms.

Similarly, the root locus plot of Fig. 3 is for a digital non-Foster RL design of a $L = -0.5$ mH inductor, as $R_{ser}$ was increased from $-500$ ohms to 0 ohms in steps of 100. Other parameters for $H(z) = H_{RL}(z)$ in Fig. 3 were $T = 1260$ ns, $R_{dac} = 1000$ ohms, $\lambda = 1$, and $R_s = 50$ ohms. At $R_{ser} = -500$ ohms, the two poles of $G(z)$ are well within the unit circle, and move outside the unit circle at $R_{ser} = 0$. The stability boundary was observed near $R_{ser} \approx -50$ ohms, with instability for $R_{ser} > -50$ ohms.

An additional root locus shown in Fig. 4 was performed on the series RC circuit to determine the effect of latency on system stability. Again, other parameters for $H(z) = H_{RC}(z)$ were $T = 1120$ ns, $C = -8$ nF, $R_{dac} = 1000$ ohms, $R_{ser} =$

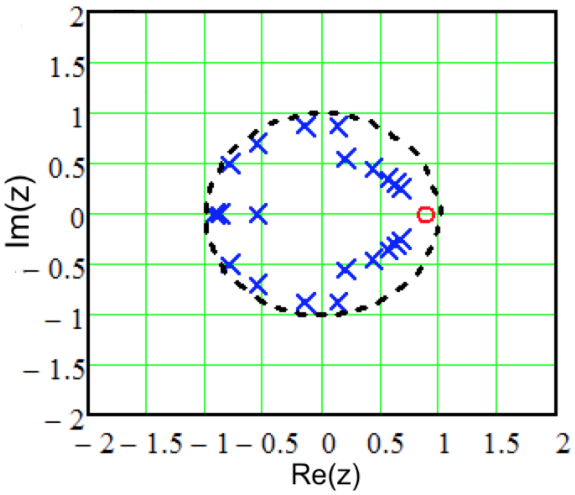


Fig. 4. Root locus stability analysis of $G(z)$ for a digital non-Foster RC circuit element with C = -8 nF, $R_s = 50$ ohms, $R_{ser} = 0$ ohms, $R_{dac}$ = 1000 ohms, $T = 1120$ ns, and latency $\lambda$ is varied from 0 to 5 clock cycles in steps of 1. Poles are denoted "X," and zeroes denoted "O."

0 ohms, and $R_s = 50$ ohms. Latency was increased from $\lambda = 0$ to $\lambda = 5$ clock cycles in integer steps, and the system poles were found to be inside the unit circle and stable for all cases. Note also, that the number of poles increases with the latency at each step. Somewhat surprisingly, as latency increased to a maximum of 5 clock cycles, the system remained stable for this particular example.

## IV. Prototype and Measurements

The NXP FRDM-K64F board shown in Fig. 5 was used to build prototypes of digital RC and RL non-Foster circuits, since this microcontroller has an on-board 16-bit ADC and 12-bit DAC. The transfer functions for the RC and RL systems as given in (2) and (3) respectively, were programmed onto the FRDM-K64F micro-controller.

First, a series RC digital discrete-time non-Foster circuit was built and measured. The system was designed to have capacitance $C = -8$ nF, and measurements were taken for two values of $R_{ser}$ within the stable region of the root locus of Fig. 2, with $R_{ser} = 0$ ohms and $R_{ser} = 50$ ohms. The measured results for $Z_{in}$ are given in Fig. 6 for $R_{ser} = 0$ ohms, and in Fig. 7 for $R_{ser} = 50$ ohms. In both figures, the solid red and dotted blue lines represent the real and imaginary parts of the theoretical input impedance $Z_{in}$, and the magenta short-dashed and cyan long-dashed lines are the real and imaginary components of the measured input impedance. In Fig. 6, at 0.05 MHz, the measured input

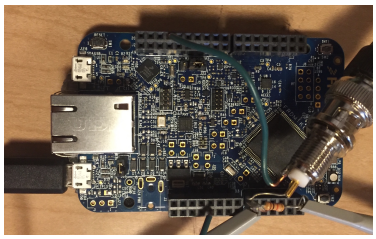

Fig. 5. Prototype digital non-Foster circuit using an NXP FRDM-K64F development board to implement the system of Fig. 1.

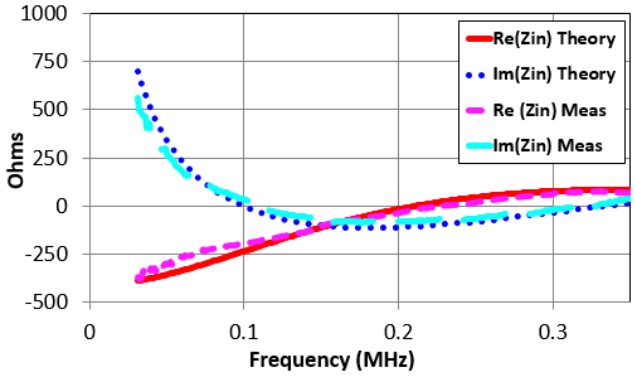


Fig. 6. Measured and theoretical input impedance $Z_{in}$ for a digital series RC circuit of Fig. 1, where $R_{ser} = 0$ ohms, $T = 1120$ ns, $C = -8$ nF, $R_{dac} = 1000$ ohms, and the latency $\tau = 1120$ ns. Solid red and dotted blue are real and imaginary parts of theoretical $Z_{in}$, and the magenta short-dashed and cyan long-dashed line are real and imaginary parts of measured $Z_{in}$.

impedance was $-302 + j273$ ohms, and the theoretical input impedance at 0.05 MHz was calculated as $-357 + j341$ ohms. In Fig. 7, at 0.05 MHz, the measured input impedance was $-234 + j294$ ohms, and the theoretical input impedance from (1) at 0.05 MHz was calculated as $-299 + j390$ ohms. Ideally, $C = -8$ nF would be $j398$ ohms at 0.05 MHz. In Fig. 6 and Fig. 7, a period of 1120 ns was used, corresponding to a sampling frequency of approximately 893 kHz, an external DAC resistance of $R_{dac} = 1000$ ohms was added, and processing time plus ADC and DAC conversion times led to an observed latency of approx. 1 clock cycle. In both figures, the shape of the reactance curve, Im($Z_{in}$), at low frequency has the expected form, exhibiting the predicted change in sign due to the negative capacitance value.

Next, a series RL digital discrete-time non-Foster circuit was built and measured. The system was designed to have inductance $L = -0.5$ mH, and measurements were taken for two values of $R_{ser}$ within the stable region of the root locus of Fig. 3, with $R_{ser} = -50$ ohms and $R_{ser} = -100$ ohms. The measured results for $Z_{in}$ are given in Fig. 8 for $R_{ser} = -50$ ohms, and in Fig. 9 for $R_{ser} = -100$ ohms. In both fig-

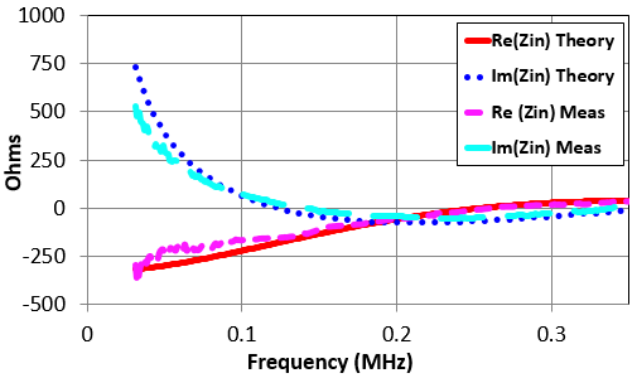


Fig. 7. Measured and theoretical input impedance $Z_{in}$ for a digital series RC circuit of Fig. 1, where $R_{ser} = 50$ ohms, $T = 1120$ ns, $C = -8$ nF, $R_{dac} = 1000$ ohms, and the latency $\tau = 1120$ ns. Solid red and dotted blue are real and imaginary parts of theoretical $Z_{in}$, and the magenta short-dashed and cyan long-dashed line are real and imaginary parts of measured $Z_{in}$.

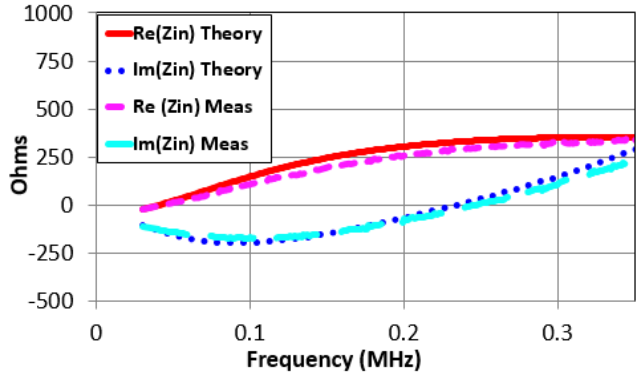


Fig. 8. Measured and theoretical input impedance $Z_{in}$ for a digital series RL circuit of Fig. 1, where $R_{ser} = -50$ ohms, $T = 1260$ ns, $L = -0.5$ mH, $R_{dac} = 1000$ ohms, and the latency $\tau = 1260$ ns. Solid red and dotted blue are real and imaginary parts of theoretical $Z_{in}$; the magenta short-dashed and cyan long-dashed line are real and imaginary components of measured $Z_{in}$.

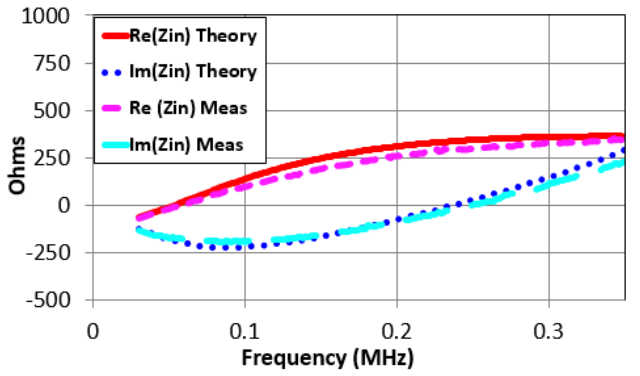


Fig. 9. Measured and theoretical input impedance $Z_{in}$ for a digital series RL circuit of Fig. 1, where $R_{ser} = -100$ ohms, $T = 1260$ ns, $L = -0.5$ mH, $R_{dac} = 1000$ ohms, and the latency $\tau = 1260$ ns. Solid red and dotted blue are real and imaginary parts of theoretical $Z_{in}$; the magenta short-dashed and cyan long-dashed line are real and imaginary components of measured $Z_{in}$.

ures, the solid red and dotted blue lines represent the real and imaginary parts of the theoretical input impedance $Z_{in}$, and the magenta short-dashed and cyan long-dashed lines are the real and imaginary components of the measured input impedance. In Fig. 8, at $0.05$ MHz, the measured input impedance was $13 - j143$ ohms , and the theoretical input impedance from (1) at $0.05$ MHz was calculated as $20 - j157$ ohms. Ideally, $L = -0.5$ mH would be $-j157$ ohms at $0.05$ MHz. In Fig. 9, at $0.05$ MHz, the measured input impedance was $-23 - j174$ ohms, and the theoretical input impedance at $0.05$ MHz was calculated as $-13 - j182$ ohms. In Fig. 8 and Fig. 9, $T$=1260 ns, corresponding to 794 kHz sampling frequency, $R_{dac} = 1000$ ohms, and the observed latency was approx. 1 clock cycle. In both figures, the shape of the reactance curve, Im($Z_{in}$), at low frequency has the expected downward-sloping form, exhibiting the predicted change in sign due to the negative inductance value.

## V. Conclusion

Stability theory, root locus plots, and prototype measurements of Thévenin-form RC and RL digital non-Foster circuits were presented. Prototype measurements confirmed stable operation for digital non-Foster RC and RL circuits, with observed negative capacitance and negative inductance, respectively. Measurements were taken at several different values of series resistance within the predicted stable range of $R_{ser}$, with latency of $\lambda = 1$ clock cycle. The root locus methods are shown to be an effective tool in determining stable operation for digital non-Foster RC and RL implementations, enabling adoption in future applications such as acoustic devices, metamaterials, and electrically-small antennas.

## References


[1] R. Fleury, D. Sounas, and A. Alù, "An invisible acoustic sensor based on parity-time symmetry," *Nature Communications*, vol. 6:5905, pp. 1–7, Jan. 2015.

[2] P.-Y. Chen, C. Argyropoulos, and A. Alù, "Broadening the cloaking bandwidth with non-Foster metasurfaces," *Phys. Rev. Lett.*, vol. 111, p. 233001, Dec. 2013.

[3] M. M. Jacob, J. Long, and D. F. Sievenpiper, "Noise in non-Foster antenna matching circuits," in *Antennas and Propagation Society International Symposium (APSURSI), 2013 IEEE*, Jul. 2013, pp. 2205–2206.

[4] T. P. Weldon and R. S. Adams, "A digital discrete-time non-Foster approach to broadband fast-wave microstrip lines," in *Advanced Electromagnetic Materials in Microwaves and Optics (METAMATERIALS), 2015 9th International Congress on*, Sep. 2015, pp. 322–324.

[5] N. Zhu and R. W. Ziolkowski, "Active metamaterial-inspired broadbandwidth, efficient, electrically small antennas," *IEEE Antennas Wireless Propag. Lett.*, vol. 10, pp. 1582–1585, 2011.

[6] F. Albarracín-Vargas, D. Segovia-Vargas, and V. Gonzalez-Posadas, "Non-Foster matching network for a small, bladetype monopole in the VHF band," in *Antennas and Propagation USNC/URSI National Radio Science Meeting, 2015 IEEE Int. Symp. on*, Jul. 2015, pp. 1396–1397.

[7] C. Robey, Frank, M. Hancock, Timothy, and B. Stahl, Gregory, "Digital matching of a radio frequency antenna," published on WIPO patentscope.wipo.int as WO2016028354 on Feb. 25, 2016, International Patent Application No. PCT/US2015/033742 filed Jun. 2, 2015.

[8] P. Cruz, N. B. Carvalho, and K. A. Remley, "Designing and testing software-defined radios," *IEEE Microw. Mag.*, vol. 11, no. 4, pp. 83–94, Jun. 2010.

[9] S. Hrabar, "Active non-Foster metamaterials: From intriguing background physics to real-world application," in *Advanced Electromagnetic Materials in Microwaves and Optics (METAMATERIALS), 2013 7th International Congress on*, Sep. 2013, pp. 601–603.

[10] S. Saadat, M. Adnan, H. Mosallaei, and E. Afshari, "Composite metamaterial and metasurface integrated with non-Foster active circuit elements: A bandwidth-enhancement investigation," *IEEE Trans. Antennas Propag.*, vol. 61, no. 3, pp. 1210–1218, Mar. 2013.

[11] E. Ugarte-Munoz, S. Hrabar, D. Segovia-Vargas, and A. Kiricenko, "Stability of non-Foster reactive elements for use in active metamaterials and antennas," *IEEE Trans. Antennas Propag.*, vol. 60, no. 7, pp. 3490–3494, Jul. 2012.

[12] S. D. Stearns, "Stable band-pass non-Foster circuits," in *2015 IEEE International Symposium on Antennas and Propagation USNC/URSI National Radio Science Meeting*, Jul. 2015, pp. 1386–1387.

[13] T. P. Weldon, J. M. C. Covington, K. Smith, and R. S. Adams, "Performance of digital discrete-time implementations of non-Foster circuit elements," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2015, pp. 2169–2172.

[14] T. P. Weldon, "Digital discrete-time non-Foster circuits and elements," published on WIPO patentscope.wipo.int as WO2015164866 on Oct. 29, 2015, International Patent Application No. PCT/US2015/27789 filed Apr. 27, 2015.

[15] T. P. Weldon, J. M. C. Covington, K. Smith, and R. S. Adams, "Stability conditions for a digital discrete-time non-Foster circuit element," in *2015 IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Jul. 2015.

[16] P. J. Kehoe, K. K. Steer, and T. P. Weldon, "Thevenin forms of digital discrete-time non-Foster RC and RL circuits," in *2016 IEEE Antennas and Propagation Society International Symposium (APSURSI)*, Jun. 2016, pp. 191–192.

[17] C. Phillips and H. Nagle, *Digital Control System Analysis and Design*. Prentice-Hall, 1990.