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Experimental Results for a Successive Detection Log Video Amplifier in a Single-Chip Frequency Synthesized Radio Frequency Spectrum Analyzer

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Abstract

The scarcity of available frequency spectrum continues to motivate the development of new radio systems capable of adapting to local conditions. One approach to identifying available frequency spectrum is to employ an on-chip radio-frequency spectrum analyzer. In particular, the present article addresses the design of an experimental Successive Detection Log Video Amplifier (SDLVA) to generate logarithmic output in a frequency-synthesized single-chip spectrum analyzer. The SDLVA design includes feedback compensation for dc offset error, and is tailored to accommodate the zero-IF architecture of the spectrum analyzer without the need for large off-chip capacitors. The SDLVA was designed and fabricated in 0.5 micron CMOS. Experimental results for the SDLVA are presented showing approximately 40 dB dynamic range. Results are also given for the overall spectrum analyzer integrated circuit showing SDLVA operation for a 200 MHz spectral sweep.

1. Introduction

The explosive growth of wireless devices has fueled ever-increasing demands on available radio frequency (RF) spectrum. To address this issue, a variety of dynamic spectrum access approaches have been proposed, including cognitive radio systems, agile radio systems, and software defined radio systems [1], [2]. In such adaptive spectrum access approaches, there is a need to measure the local frequency spectrum environment. Furthermore, there is a similar need in other applications such as spectral monitoring [3].

To address such emerging applications, a single-chip CMOS frequency-synthesized radio-frequency spectrum analyzer is under development. The on-chip frequency synthesizer enables accurate and repeatable frequency measurement, although it does increase the circuit complexity and chip area. A zero-intermediate-frequency (zero-IF) architecture is chosen to simplify the radio system architecture, to minimize chip area, to avoid image-frequency problems, and eliminate the need for image-rejection filters.

To demonstrate proof-of-principle, an initial prototype of the spectrum analyzer, including the frequency synthesizer, has been developed for spectral measurements up to 200 MHz. For the reasons noted earlier, the fabricated frequency-synthesized spectrum analyzer design employs an ac-coupled zero-IF architecture. In addition, the fabricated device includes a logarithmic output for the spectrum analyzer.

The present paper primarily focuses on the design and measurement of the Successive Detection Log Video Amplifier (SDLVA) stage in the spectrum analyzer under development. The SDLVA design is tailored to accommodate the zero-IF architecture of the overall spectrum analyzer in which it is embedded. Since zero-IF architectures can suffer from large dc offset voltage problems, the SDLVA includes ac coupling and dc offset compensation feedback as outlined in [4]. However, the proposed SDLVA is implemented without the need for external off-chip capacitors. Other researchers have further outlined the requirements in a zero-IF architecture for large capacitors and very low corner frequencies for the high-pass ac-coupling [5]. Nevertheless, such restrictions are somewhat relaxed in the current application, since the spectrum analyzer does not require full demodulation of signals. Consequently, the less stringent ac-coupling considerations for the present application allow an SDLVA design without large off-chip capacitors.

Although the present article primarily addresses the SDLVA, the SDLVA is designed to be embedded in a frequency-synthesized spectrum analyzer. Therefore, the design of the overall spectrum is also outlined. In addition, measured data is also provided showing the operation of the SDLVA in the complete spectrum analyzer system.

In the following, the overall spectrum analyzer architecture is first given. Then, the SDLVA design is discussed. Finally, measured test results are presented for the SDLVA and the overall spectrum analyzer.

2. Spectrum Analyzer Architecture

Before describing the SDLVA design in the following section, it is useful to first outline the overall spectrum analyzer architecture. As illustrated in Fig. 1, the single-chip spectrum analyzer employs a zero-IF architecture with logarithmic output and a frequency-synthesized local oscillator (LO). At the left of Fig. 1, the RF input is first amplified in a low noise amplifier (LNA) before entering

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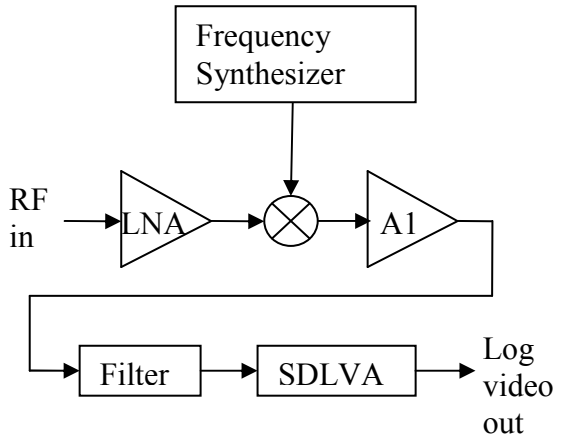

Fig. 1. Block diagram of frequency-synthesized spectrum analyzer. Spectrum analyzer input is denoted "RF in," and spectrum analyzer output is denoted "Log video out."

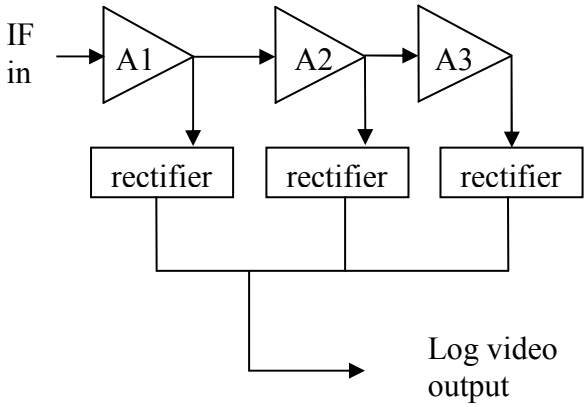

Fig. 2. Block diagram of SDLVA. SDLVA input is "IF in," and spectrum analyzer output is "Log video out."

the mixer. The frequency synthesizer at the top of the figure drives the second input port of the mixer. In the following examples, the frequency synthesizer is swept from 1.56 MHz to 200 MHz in 128 steps, spending approximately 21 milliseconds at each frequency. Since this is a zero-IF architecture, the spectrum analyzer is tuned to the same frequency as the frequency synthesizer. The output of the mixer in Fig. 1 is then amplified and filtered in IF amplifier A1. Finally, the output of the IF amplifier is applied to the input of the SDLVA to generate the logarithmic detected video output.

3. SDLVA Design

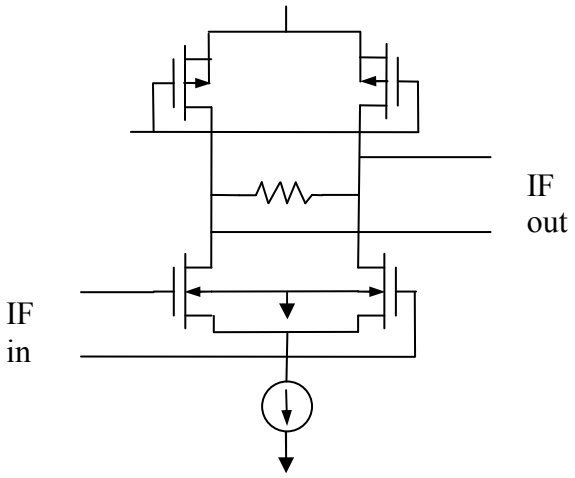

Fig. 3. Amplifier schematic

A block diagram of the SDLVA design is given in Fig 2 and is along the lines of the design in reference [4]. The IF input is amplified in three stages of differential amplifiers, A1 through A3. Each amplifier stage, A1 through A3, has differential input and output as shown in the schematic of Fig. 3. The IF input is applied to the NMOS differential pair gates, and the differential IF output is taken from the PMOS loads. An on-chip resistor adjusts the stage gain.

Each of the differential amplifier outputs in Fig. 2 drives a fully differential rectifier circuit. A single-ended to differential driver was also included on chip for the purpose of testing the SDLVA separate from the spectrum analyzer. In operation, the three stages of Fig. 2 are saturating amplifiers, driving the three rectifiers to form a piecewise approximation to generate a logarithmic output. Further details can be found in reference [4].

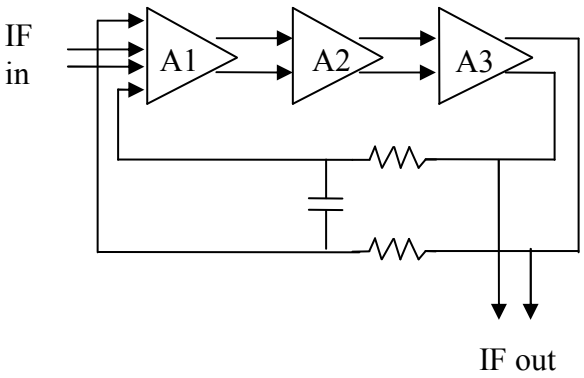

Fig. 4. Block diagram of SDLVA dc feedback offset error compensation.

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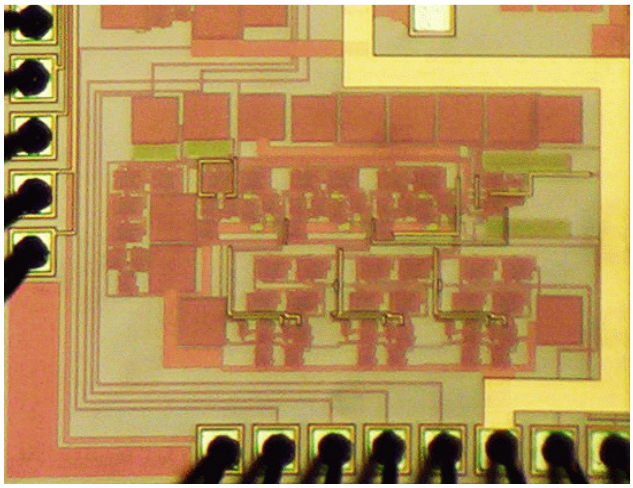

Fig.5 Photograph of SDLVA fabricated in 0.5 micron CMOS.

The three differential amplifiers of Fig. 2 are also depicted in the block diagram of Fig. 4, but with detail of the differential feedback compensation for dc offset errors. The two resistors and the capacitor comprise the dc feedback compensation. The feedback approach of Fig. 4 is described in detail in reference [4], where an off-chip 140 μF capacitor was used. As noted previously, the present design uses on-chip capacitors, since the spectrum analyzer requirements are less stringent than a receiver requiring full signal demodulation. Finally, a photograph of the fabricated DLVA is shown in Fig. 5.

4. Experimental Results

The logarithmic response of the SDLVA prototype was measured at 1MHz, and the results are plotted in Fig. 6. The 1MHz signal was varied from -60 dBm to 20 dBm while the logarithmic output was measured. As seen in Fig. 6, an approximately logarithmic response was observed between -40 dBm and 0 dBm, with a corresponding output voltage between 66 mV and 20 mV, and with a nominal slope of 1.15 mV/dB.

The measured frequency response of the SDLVA is given in Fig. 7, where the logarithmically scaled vertical axis indicates the linear video output voltage in mV peak-to-peak. The measured 3 dB bandwidth ranges from 800 kHz to 8 MHz.

Fig. 8 shows the operation of the SDLVA embedded in the overall frequency-synthesized spectrum analyzer of Fig. 1. In Fig. 8, the horizontal axis is RF input frequency, and the upper trace vertical axis is the logarithmic video output. The falling edge of the bottom trace indicates frequency synthesizer transition from 200 MHz to 0 Hz, and the rising edge indicates a frequency of 100 MHz. The large dip in the upper trace indicates the strong 180 MHz RF input test signal. The axis appears to be inverted, since

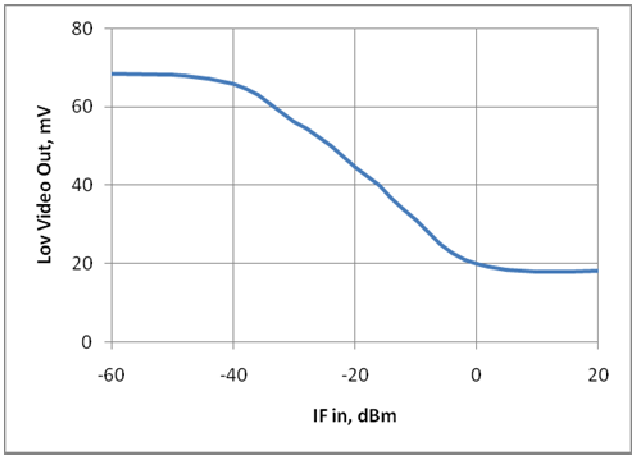

Fig. 6. SDLVA measured response for a 1 MHz input signal. Horizontal axis is IF input signal strength in dBm, vertical axis is measured log detected video output voltage.

larger signals correspond to lower voltages as given previously in Fig. 6. Also, in Fig. 5 the response at 90 MHz corresponds to a 2LO - RF mixer spurious response, and other mixer spurious responses are visible

Finally, the oscilloscope trace of Fig. 8 can be converted into a non-inverted spectral plot using the previously measured response in Fig. 6 of approximately 1.15 mV/dB. The non-inverted spectrum is shown in Fig. 9 and corresponds to the oscilloscope trace of Fig. 8.

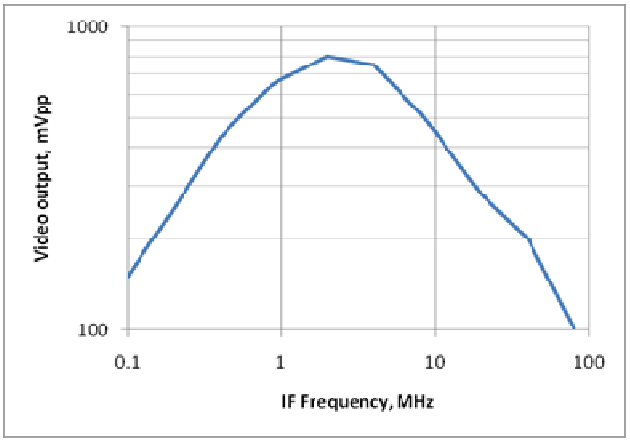

Fig. 7. SDLVA measured frequency response for a 1 MHz input signal at 12 mVpp. Horizontal axis is IF input signal frequency in MHz, vertical axis is measured linear video output voltage peak-to-peak.

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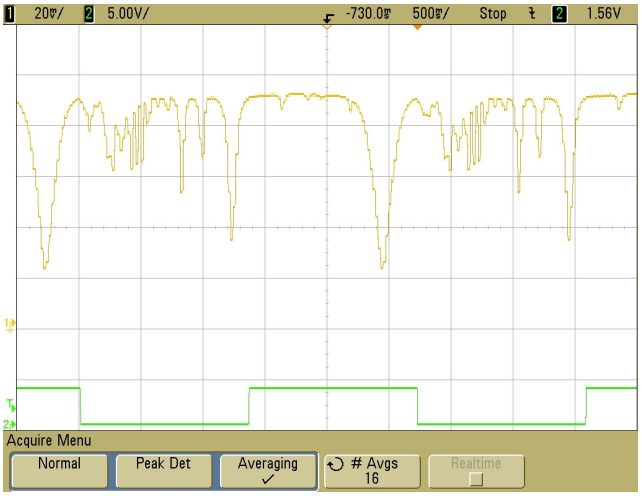

Fig. 8. Spectrum analyzer: measured spectrum of 180 MHz -10 dBm sinusoid. The Horizontal axis is RF input frequency, from 0 to 200. Large dip in upper trace indicates strong 180 MHz RF input signal (axis inverted).

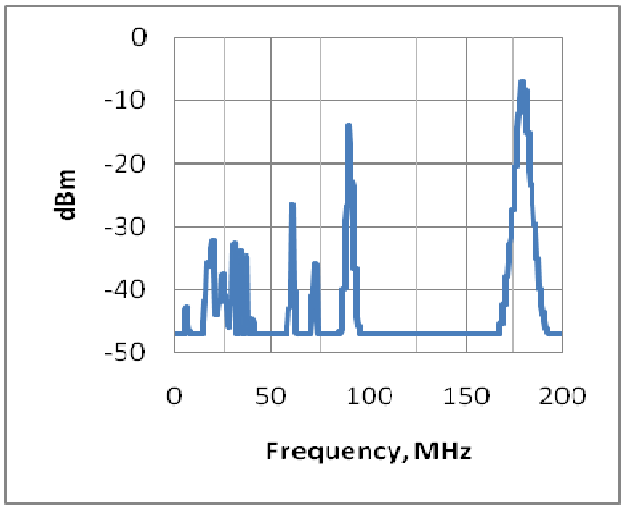

Fig. 9. Spectrum analyzer: measured spectrum of 180 MHz -10 dBm sinusoid. Horizontal axis is RF input frequency, vertical avis is logarithmic video output converted to equivalent power level in dBm.

5. Conclusion

A successive detection log video amplifier has been fabricated and tested for use in a frequency-synthesized single-chip spectrum analyzer. The SDLVA operates from 800 KHz to 8 MHz with approximately 40 dB of logarithmic signal range. The SDLVA was also demonstrated in a 250 MHz spectrum analyzer sweep.

6. Acknowledgements

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7. References

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