# Use of a Digital Non-Foster Radio Architecture for Conventional Tuning of Electrically-Small Antennas

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***Abstract*—Prior investigations of digital non-Foster antenna tuning have pointed out the similarity between these systems and SDR (software-defined radio) systems, where the SDR receiver ADC (analog-to-digital converter) and SDR DAC (digital-to-analog converter) can serve corresponding digital non-Foster circuit roles. In previous investigations, the particular focus has been on using digital non-Foster antenna impedance matching methods to overcome Wheeler-Chu limits of electrically-small antennas. However, the digital non-Foster radio architecture can also provide digital implementation of conventional impedance matching of electrically-small antennas. The advantage is that the impedance matching is accomplished in software without the need for external matching circuitry, allowing digital tuning of the antenna to desired frequency bands. Although such conventional impedance matching would not provide the bandwidth enhancement of non-Foster matching, it may be useful in providing some degree of preselection filtering for narrowband applications. Simulation results illustrate the proposed digital impedance-matching approach, and are compared to a conventional passively-matched electrically-small antenna at 75 MHz.**

## I. Introduction

Despite considerable progress in the evolution of SDR (software-defined radio), the Wheeler-Chu bandwidth limit of electrically-small antennas remains as a fundamental impediment to practical implementations of wideband mobile SDR much below a few hundred MHz [1], [2]. Much progress has been made in the design of non-Foster antenna matching networks to overcome these limits [3]–[5]. More recently, digital non-Foster impedance matching of electrically small antennas has also been proposed, having the added benefit of the potential for an adaptive software-programmable approach [6]. Nevertheless, passive matching networks may be suitable for stability enhancement, for narrowband applications, or for use in systems where narrowband antenna tuning may offer useful preselection filtering to suppress receiver blocking by strong interfering signals at nearby frequencies [7].

Therefore, a digital non-Foster software-defined radio architecture is considered for digital implementation of conventional passively-matched electrically-small antennas. While the radio architecture is essentially the same as for digital non-Foster implementations, it is here used to implement digital equivalents of more conventional passive-matching networks with non-negative elements. Two key features of the proposed digital approach are the innate programability of the antenna tuning, and the inherent stability of the analog passive matching networks being replaced. In essence, the proposed approach replaces a conventional analog series-/parallel RLC (series/parallel resistor-inductor-capacitor) antenna impedance matching network with its digital equivalent. Lastly, the implementation of the proposed digital non-Foster antenna tuning in an existing SDR may simply require an added filter functionality $H(z)$ coupling between the SDR receiver signal path and SDR transmitter signal path.

## II. Digital Non-Foster Antenna Impedance Match

A block diagram of proposed digital non-Foster SDR approach is illustrated in Fig. 1, where a 0.15 m long, 1.5 cm radius monopole antenna drives the digital non-Foster front end of an SDR, and where the digital non-Foster front end is programmed to emulate the analog equivalent on the right (*but with no negative elements,* and no non-Foster behavior). The digital non-Foster front end provides the antenna impedance matching. At 75 MHz ($\omega_\circ = 150\pi \times 10^6$), the antenna has capacitance $C_{ant} \approx 6.6$ pF and radiation resistance $R_{ant} \approx 3.2$ ohms, with $Q_{ant} \approx 1/(\omega_\circ R_{ant} C_{ant}) = 100$, and a Wheeler-Chu antenna size parameter $ka = 0.24$ for $k = \omega_\circ/c = \omega_\circ/3 \times 10^8$ and $a = 0.15$ m. The corresponding predicted Wheeler-Chu 6 dB bandwidth limit would then be $B \approx 2[\sqrt{3}/(ka)^3 + \sqrt{3}/(ka)]^{-1} = 1.5\%$ from [1], assuming an antenna efficiency of 100%.

In the digital non-Foster front end within the left-hand dashed box of Fig. 1, the ADC with clock period $T$ converts the voltage from the antenna $v_{nf}(t)$ into digital signal $v_{nf}[n] = v_{nf}(nT)$, and $v_{nf}[n]$ is passed on to the SDR receiver. The signal $v_{nf}[n]$ corresponds to the voltage $v_{nf}(t)$

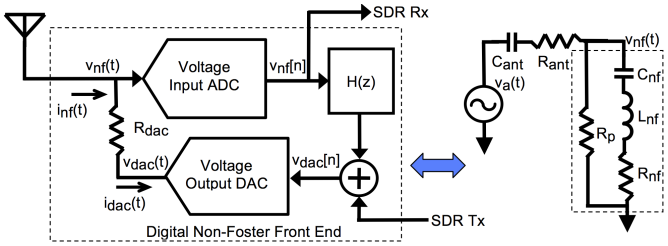


Fig. 1. Proposed digital non-Foster radio architecture, showing digital non-Foster front end in dashed box on left, and equivalent conventional series/parallel-RLC impedance matching to an electrically small antenna in dashed box on right. On the left, the digital non-Foster front end provides conventional impedance matching, outputting the digitized signal $v_{dac}[n]$ to the remainder of the SDR for processing, "SDR Rx." Provision for SDR transmitter signal "SDR Tx" is shown, presumed zero in this paper.

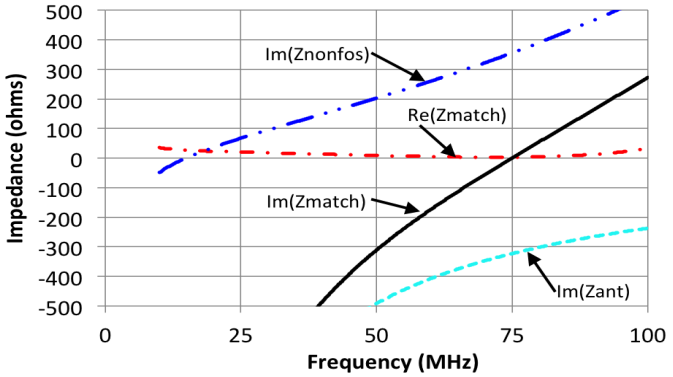


Fig. 2. Simulation results for digital series/parallel-RLC impedance-matched 0.15 m monopole antenna, showing real and imaginary parts of matched antenna denoted as Re(Zmatch) and Im(Zmatch) respectively, showing imaginary part of unmatched antenna impedance denoted as Im(Zant), and showing imaginary part of digital non-Foster front end denoted Im(Znonfos). Note that the digital non-Foster front end here implements a series/parallel-RLC *with positive elements,* rather than a non-Foster impedance.

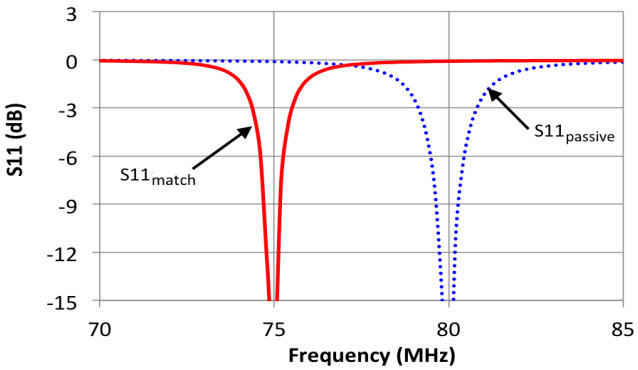


Fig. 3. Simulation results for series/parallel-RLC impedance-matched 0.75 m monopole antenna, showing return loss of matched antenna denoted as $S_{11match}$ and return loss of the same antenna passively-matched with a single inductor denoted as $S_{11passive}$. Note that the digital series/parallel-RLC match has better than 6 dB return loss from approx. 74.6 to 75.2 MHz, similar to the passively-matched bandwidth from 79.4 to 80.4 MHz (slightly larger bandwidth as expected at this nearby higher frequency). Non-Foster bandwidth enhancement is absent, since *all positive elements* were used.

on the equivalent analog circuit on the right. Next, digital filter $H(z)$ forms the convolution $v_{dac}[n] = h[n] * v_{nf}[n]$, where $H(z)$ is the z-transform of $h[n]$. Lastly, the DAC converts $v_{dac}[n]$ into an analog signal $v_{dac}(t)$, and the input current is determined by $i_{dac}(t) = [v_{nf}(t) - v_{dac}(t)]/R_{dac}$. As described in [8], the impedance of the digital non-Foster matching circuit in the dashed box of Fig. 1 as seen by the antenna is then

$$Z_{in}(s) = \frac{V_{nf}(s)}{I_{nf}(s)} \approx \left. \frac{sTR_{dac}}{sT - H(z)\,(1 - z^{-1})\,e^{-s\tau}} \right|_{z=e^{sT}}, \quad (1)$$

for signals without aliasing and below $1/(2T)$ Hz.

Next, $H(z)$ is determined from the equivalent series/parallel-RLC impedance of the right-hand dashed box of Fig. 1, where again, *the circuit elements are all presumed to be positive* for the present paper. The impedance of the circuit is $Z_{nf}(s) = V_{nf}(s)/I_{nf}(s) = (s^2 L_{nf} C_{nf} + sR_{nf} C_{nf} + 1)/(sC_{nf})$, or $I_{nf}(s) = sC_{nf}\, V_{nf}(s)/(s^2 L_{nf} C_{nf} + sR_{nf} C_{nf} + 1)$. Since $i_{nf}(t) = [v_{nf}(t) - v_{dac}(t)]/R_{dac}$, then $I_{nf}(s) = I_{dac}(s) = [V_{nf}(s) - V_{dac}(s)]/R_{dac}$. Substituting for $I_{nf}(s)$, then solving for $H(s) = V_{dac}(s)/V_{nf}(s)$, and lastly taking the bilinear transform of $H(s)$ gives

$$H_{RLC}(z) = \left. \frac{s^2 L_{nf} C_{nf} + sC_{nf}(R_{nf} - R_{dac}) + 1}{s^2 L_{nf} C_{nf} + sC_{nf} R_{nf} + 1} \right|_{s=\frac{2}{T}\frac{z-1}{z+1}}. \quad (2)$$

The parallel resistance $R_p$ is implemented by adding $H_{Rp}(z) = 1 - R_{dac}/(R_p || R_{dac})$ to $H_{RLC}(z)$ to produce the total $H(z) = H_{RLC}(z) + H_{Rp}(z)$.

## III. Simulation Results and Conclusion

The circuit on the left of Fig. 1 was simulated in the Keysight ADS large-signal S-parameter simulator. with digital non-Foster parameters $C_{nf} = 250$ pF, $L_{nf} = 665$ nH, $R_{nf} = 15$ ohms, and $R_p = 500$ ohms, for $T = 2.5$ ns and $R_{dac} = 1000$ ohms, and negligible latency $\tau \approx 0$. Fig. 2 shows the real (red dash-dot) and imaginary (black solid) parts of the matched antenna impedance Fig. 1. The imaginary part of the uncompensated antenna (cyan dashed) and the imaginary part (blue dash-dot-dot) of the digital non-Foster front-end impedance $Z_{in}$ are also shown. Fig. 3 shows the return loss of the matched antenna (solid red), along with the return loss of the antenna passively matched with a single 600 nH inductor.

Since the objective was to provide the digital equivalent of a passively matched antennna, there is no bandwidth enhancement visible in Fig. 2, as there would be if a digital non-Foster impedance match was desired. Comparison of the passive and digital non-Foster impedance matches in Fig. 2, show that the digital non-Foster radio architecture of Fig. 1 *is also capable of digitally implementing a passively matched electrically-small antenna.* The advantage of the proposed method is the potential for software implementation of adaptively matched electrically-small antennas in SDR radio designs.

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