Bilinear Transform Approach for Wideband Digital Non-Foster Matching of Electrically-Small Antennas

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***Abstract*—A digital non-Foster design approach is presented for wideband matching of an electrically-small monopole antenna using the bilinear transform. A digital negative capacitance in a series/parallel-RLC digital non-Foster matching network is used to increase bandwidth by cancelling a large portion of the capacitive reactance of an electrically-short monopole. A digitally-implemented positive inductance tunes the center frequency, eliminating residual reactance. A second digital resistor in parallel enhances stability. Simulation results show wideband impedance match of a 0.75 m monopole, with better than 6 dB return loss from 19.0 to 23.8 MHz, compared to a conventional passively-matched bandwidth of 20.2 to 20.7 MHz and a Wheeler-Chu limit of 3.3 percent for ka=0.314.**

I. Introduction

The bandwidth of passively-matched electrically-small antennas are severely constrained by the Wheeler-Chu limit as summarized in [1]. Non-Foster analog circuits such as negative capacitors have recently been used to overcome these limits, with recent successful implementations as in [2], [3], avoiding potential instability [4]. More recently, the digital non-Foster circuits in [5], [6] offer potential for adaptive solutions addressing impedance variations noted in [7], and for leveraging advantages inherent in digital technologies such as software-defined radio [8].

Although earlier results in [6] consider adaptive digital non-Foster RC impedance matching of a simple RC model of an electrically-small antenna, stable matching to more complex Keysight ADS "AntLoad" monopole antenna models remained challenging. Therefore, a digital non-Foster series/parallel-RLC (series/parallel resistor-inductor-capacitor) impedance matching is proposed below, providing overall stability when simulated with an ADS monopole antenna model. In this, the digital RLC circuit combined with the antenna is designed to result in a net positive capacitance and positive inductance with non-decreasing reactance in the vicinity of the tuned operating frequency. Though a higher-order digital matching network could have more potential for instability than the first-order method in [6], simulation experience with the new digital RLC approach anecdotally seems to more readily produce stable digital non-Foster antenna-matching designs.

II. Digital Non-Foster Antenna Impedance Match

The proposed approach is illustrated in Fig. 1, where the left side of the figure shows an input $v_{in}(t)$ applied to a 1:1 ideal transformer that couples the impedance of a 0.75 m long, 7.5 cm radius, monopole antenna in series with the digital non-Foster impedance matching circuit shown in the left-hand dashed box. (The ideal transformer simply converts the single-terminal antenna model into two terminals.) At a design frequency of 20 MHz ($\omega_0 = 40\pi \times 10^6$), the equivalent circuit on the right of Fig. 1 has antenna capacitance $C_{ant} \approx 33.7$ pF and radiation resistance $R_{ant} \approx 4.5$ ohms, with $Q_{ant} \approx 1/(\omega_0 R_{ant} C_{ant}) = 52$, $ka = 0.314$ for $k = \omega_0/c = \omega_0/(3 \times 10^8)$, and Wheeler-Chu bandwidth limit of $B = (s-1)[\sqrt{s}/(k\,a)^3 + \sqrt{s}/(k\,a)]^{-1} = 3.3\%$ for VSWR (voltage standing wave ratio) $s = 3$ from [1] for antenna efficiency $\eta = 100\%$, where $B\eta = B$.

In the digital non-Foster circuit in the left-hand dashed box of Fig. 1, voltage $v_{nf}(t)$ is converted into a digital signal by the ADC with clock period T to form $v_{nf}[n] = v_{nf}(nT)$. Next, signal processing block $H(z)$ performs the convolution $v_{dac}[n] = h[n] * v_{nf}[n]$, where $H(z)$ is the z-transform of $h[n]$. Lastly, the DAC converts $v_{dac}[n]$ into an analog signal $v_{dac}(t)$. As described in [5], the impedance of the digital non-Foster matching circuit in the dashed box of Fig. 1 is then

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \left. \frac{sTR_{dac}}{sT - H(z)\,(1-z^{-1})\,e^{-s\tau}} \right|_{z=e^{sT}}, \qquad (1)$$

for signals without aliasing and below $1/(2T)$ Hz.

Step 1: The first step in the proposed overall design approach is to determine the digital series/parallel-RLC parameters (R_{nf}, L_{nf}, C_{nf}, and R_p in Fig. 1) such that the series/parallel-RLC combined with the antenna yields a net positive capacitance and net positive inductance. The net positive inductance and capacitance are used to produce a stable non-decreasing reactance in the vicinity of the tuned operating frequency, ω_0. To achieve this, set $R_{nf} = 0$, and let $Q_d \approx 1/B_d$, where $0 < Q_d < Q_{ant}$, and Q_d is the

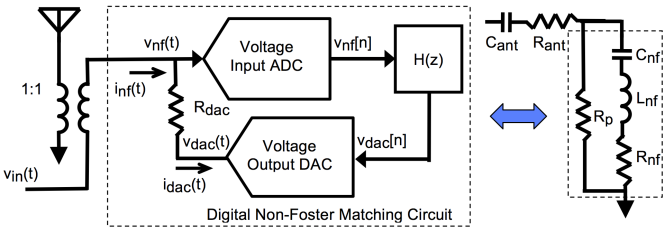

Fig. 1. Proposed digital non-Foster series/parallel-RLC approach to impedance matching an electrically small antenna. On the left, input $v_{in}(t)$ the antenna impedance through a 1:1 ideal transformer is coupled in series with the digital non-Foster impedance matching circuit in the dashed box. The equivalent circuit for design purposes is shown on the right with antenna capacitance C_{ant}, antenna radiation resistance R_{ant}, and digital non-Foster series/parallel-RLC parameters R_{nf}, L_{nf}, C_{nf}, and R_p.

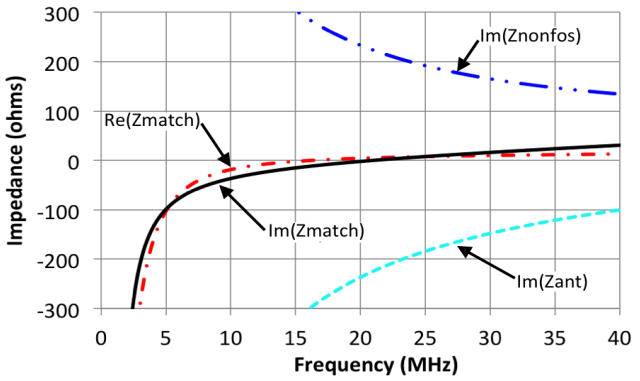

Fig. 2. Simulation results for digital non-Foster series/parallel-RLC impedance matched 0.75 m monopole antenna, showing real and imaginary parts of matched antenna denoted as Re(Zmatch) and Im(Zmatch) respectively, showing imaginary part of unmatched antenna impedance denoted as Im(Zant), and showing imaginary part of digital non-Foster series/parallel-RLC impedance denoted Im(Znonfos). Note non-decreasing Im(Zmatch) passing through 0 at 20 MHz.

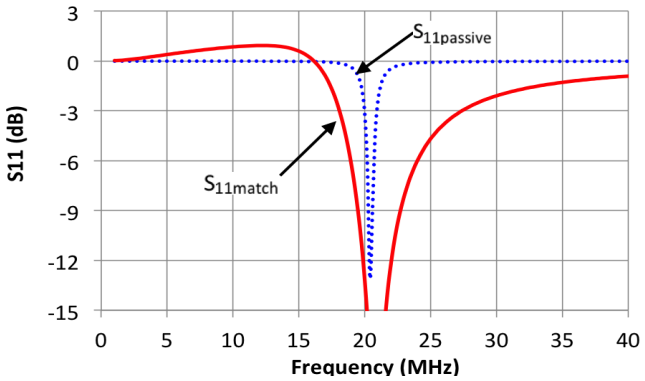

Fig. 3. Simulation results for digital non-Foster series/parallel-RLC impedance matched 0.75 m monopole, showing return loss of matched antenna denoted as $S_{11match}$ and return loss of the same antenna passively-matched with a single inductor denoted as $S_{11passive}$. Note that the digital non-Foster series/parallel-RLC match has better than 6 dB return loss from 19.0 to 23.8 MHz, compared to passively-matched bandwidth from 20.2 to 20.7 MHz.

desired quality factor after negative capacitance C_{nf} is used to cancel some portion of C_{ant} (setting $L_{nf} = 0$ when computing Q_d). Further, presume that the primary function of positive inductance L_{nf} is to cancel the residual negative reactance of C_{ant} in series C_{nf}. With C_{nf} in series with C_{ant}, then $Q_d = [1/(\omega_0 C_{ant}) + 1/(\omega_0 C_{nf})]/R_{ant}$. Since $1/(\omega_0 C_{ant}) = Q_{ant} R_{ant}$, substituting yields $Q_d = Q_{ant} + Q_{ant} C_{ant}/C_{nf}$, so that $C_{nf} = C_{ant} Q_{ant}/(Q_d - Q_{ant})$. For the current example, let $Q_d = Q_{ant}/14.4 = 3.6$, then $C_{nf} = 52\, C_{ant}/(3.6 - 52) \approx -36.2$ pF. At resonance, the magnitudes of the *total* capacitive reactance and the inductive reactance both must equal $Q_d R_{ant}$, so $L_{ant} = Q_d R_{ant}/\omega_0 = 129$ nH.

Step 2: The second step in the design procedure is to determine $H(z)$ for the digital non-Foster series/parallel-RLC circuit in the dashed box of Fig. 1. To find $H(z)$, note that the equivalent series/parallel-RLC impedance of the right-hand dashed box of Fig. 1 is $Z_{nf}(s) = V_{nf}(s)/I_{nf}(s) = (s^2 L_{nf} C_{nf} + s R_{nf} C_{nf} + 1)/(s C_{nf})$, or $I_{nf}(s) = s C_{nf}\, V_{nf}(s)/(s^2 L_{nf} C_{nf} + s R_{nf} C_{nf} + 1)$. Since $i_{nf}(t) = [v_{nf}(t) - v_{dac}(t)]/R_{dac}$, then $I_{nf}(s) = [V_{nf}(s) - V_{dac}(s)]/R_{dac}$. Substituting for $I_{nf}(s)$, then solving for $H(s) = V_{dac}(s)/V_{nf}(s)$, and lastly taking the bilinear transform of $H(s)$ gives

$$H_{RLC}(z) = \left. \frac{s^2 L_{nf} C_{nf} + s C_{nf}(R_{nf} - R_{dac}) + 1}{s^2 L_{nf} C_{nf} + s C_{nf} R_{nf} + 1} \right|_{s=\frac{2}{T}\frac{z-1}{z+1}} . \quad (2)$$

It is straightforward to show that the parallel resistance R_p can implemented by adding a $H_{Rp}(z) = 1 - R_{dac}/(R_p || R_{dac})$ to $H_{RLC}(z)$ for the total $H(z) = H_{RLC}(z) + H_{Rp}(z)$.

Step 3: The last step in the design process is to simulate the resulting design and adjust the values of L_{nf} and R_{nf}. First, the value of L_{nf} is adjusted so that the total reactance seen at $v_{in}(t)$ equals zero at the design frequency ω_0. Secondly, the resistances R_{nf} and R_p are adjusted such that the total resistance seen at $v_{in}(t)$ equals R_{ant} at the design frequency ω_0. These adjustments can compensate for parasitic resistance and for inevitable frequency warping of the bilinear transform. The final adjusted parameters for (2) were $C_{nf} = -36.2$ pF, $L_{nf} = 70$ nH, $R_{nf} = 25$ ohms, and $R_p = 7,000$ ohms, for $T = 1$ ns, $R_{dac} = 200$ ohms, and negligible latency $\tau \approx 0$.

III. Simulation Results and Conclusion

The circuit on the left of Fig. 1 was simulated in the Keysight ADS large-signal S-parameter simulator. Fig. 2 shows the real (red dash-dot) and imaginary (black solid) parts of the matched antenna impedance as seen from $v_{in}(t)$ of Fig. 1. For comparison, the imaginary part of the uncompensated antenna (cyan dashed) and imaginary part (blue dash-dot-dot) of the digital non-Foster impedance Z_{nf} are also shown. Fig. 3 shows the return loss of the matched antenna (solid red) as seen from $v_{in}(t)$ in Fig. 1, along with the return loss of the antenna passively matched with a single 1800 nH inductor. Clearly, the 22% bandwidth of the digital non-Foster matched antenna greatly exceeds the simulated 2.4% bandwidth of the passive match and the Wheeler-Chu limit of 3.3 % for $ka = 0.314$.

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