Search-Based Design of Digital Non-Foster Antenna Match for High-Speed Low-Impedance Converters

Vinit A. Katariya and Thomas P. Weldon
Department of Electrical and Computer Engineering
University of North Carolina at Charlotte
Charlotte, NC, USA

Abstract—Previous design procedures for low-frequency digital non-Foster circuits are most effective when high input impedance analog-to-digital converters are employed. However, these earlier design methods did not include the effects of potentially low impedances of high-frequency ADCs (analog-to-digital converters). Therefore, we propose a new search-based design procedure for digital non-Foster antenna-matching circuits using low-impedance converters. An example of the new design method is presented, with simulation results showing effective impedance matching of a 10 MHz electrically-small antenna using a digital non-Foster circuit and a low-impedance converter.

I. INTRODUCTION

The bandwidth of passively matched electrically-small antennas are constrained by the Wheeler-Chu limit [1]. A number of analog and digital non-Foster approaches have been proposed [2]–[4] to overcome the Wheeler-Chu limit. However, prior digital non-Foster design methods did not incorporate the effects of low impedances of high-frequency ADCs (analog-to-digital converter). Therefore, we propose a new search-based design procedure for digital non-Foster impedance matching of antennas, where low-impedance high-speed converters are employed.

II. DIGITAL NON-FOSTER APPROACH

A block diagram of a system for impedance matching of an antenna is shown in Fig. 1. The impedance of the digital non-Foster circuit in the large dashed box is in series with antenna impedance, \( Z_A(s) \). A test source with impedance, \( R_T = Re(Z_A(s)) \) is included for measuring s-parameters.

The voltage at the input of the non-Foster circuit, \( V_{nf}(s) \), is digitized by the ADC with input resistance \( R_{adc} \) and sampling time, \( T = 10 \text{ ns} \) to form \( V_{nf}[n] \). The current of the digital non-Foster circuit is, \( I_{nf}(s) = V_{nf}(s)/R_{adc} + \left[ V_{nf}(s) - V_{dac}(s) \right]/\left[ R_{io} + R_{dac} \right] \). The impedance of the digital non-Foster circuit, \( Z_{nf}(s) = V_{nf}(s)/I_{nf}(s) \), is

\[
Z_{nf}(s) \approx \frac{sTR_{adc}(R_{io} + R_{dac})}{sT(R_{adc} + R_{io} + R_{dac}) - R_{adc}H(z)(1 - z^{-1})} \bigg|_{z = e^{-T}} \quad (1)
\]

where \( V_{nf}(s) \) is sampled without aliasing [4]. For the proposed search-based design procedure \( H(z) \) is presumed to be:

\[
H(z) = \frac{b_0z^2 + b_1z + b_2}{z^2 + a_1z + a_2} \quad (2)
\]

where \( b_0, b_1, b_2, a_1, a_2 \) are real numbers.

III. SEARCH-BASED STABLE DESIGN APPROACH

As noted earlier, prior digital non-Foster design methods did not include effects of low-impedance (50Ω) converters. Therefore, we propose a search-based design method to find the parameters \( b_0, b_1, b_2, a_1, a_2 \) to match the antenna impedance. The search criteria is minimum error in the desired non-Foster impedance, \( Z_{nf}(s) \), subject to the constraint of a stable system.

The flowchart in Fig. 2 describes the basic search procedure. The coefficients in (2) are searched over a range determined by the application, in the present case -25 to 25, step size 0.25. Then, each set of coefficients is checked for stability according to the characteristic equation described later.

After checking for stability, coefficient sets with real part \( Re\{Z_{nf}(s)\} \) outside the range of -3 to 3 are discarded, to preserve antenna efficiency. Next, a heuristic error measure \( E = E^2(j\omega_1) + E^2(j\omega_2) + E^2(j\omega_3) \) for three frequencies is tested for each parameter set, where

\[
E(s) = \frac{100|Im(Z_{nf}(s) - Z_d(s))|}{|Im(Z_d(s))|} + \frac{100|Re(Z_{nf}(s) - Z_d(s))|}{25|Re(Z_d(s))|} \quad (3)
\]

\( Im() \) and \( Re() \) denote real and imaginary parts, and \( Z_d(s) \) is the desired non-Foster matching impedance. Lastly, the minimum error solution is retained. A second pass is then done using a step size of 0.01 to refine the solution.

As noted above, the search-based method tests each set of coefficients for stability using poles of the characteristic equation of the system in Fig. 1, along the lines of [5]. The

---

Fig. 1. Block diagram of digital non-Foster antenna matching circuit, with digital non-Foster approach of [4] modified to add low-impedance \( R_{adc} \) and \( R_{dac} \), with antenna impedance \( Z_A(s) \) and test source shown. Right: schematic illustrating desired digital non-Foster equivalent series-RLC \( R_{nf}, C_{nf}, \) and \( I_{nf} \) for antenna impedance match.
system poles can be shown to be from the denominator of
\[
\frac{C(z)}{R(z)} = \frac{H(z)(\frac{1}{R_{io} + R_{dac}})Z_t(z)}{1 - H(z)(\frac{1}{R_{io} + R_{dac}})Z_t(z)}
\]
where \(Z_t(z) = Z_A(s)||R_{adc}||(R_{io} + R_{dac})\), and \(C(z)/R(z)\) is related to the closed loop response of the system of Fig. 1.

IV. SIMULATION RESULTS

This section presents simulation results for the wideband impedance matching of an electrically-small antenna with a digital non-Foster circuit including the effects of low-impedance converters. Below, we first describe how we obtain the desired impedance \(Z_d(s)\) for (3). Then, we present simulation results showing that our search-based design of Fig. 3 provides a wideband non-Foster match to an electrically-small antenna.

First, the desired impedance \(Z_d(s)\) of the series RLC circuit in Fig. 1 to provide a wideband non-Foster match to a 2 m long, 2 cm radius, electrically-small monopole at 10 MHz is obtained. At 10 MHz, the antenna impedance is \(\approx 5 - j479 \Omega\) (\(\approx 33.2 \text{ pF}\)). Based on the antenna impedance, the desired non-Foster matching impedance is determined using the procedure described in [4], for our example \(C_{nf} = -37 \text{ pF}, L_{nf} = 790 \text{ nH}\) and \(R_{nf} = 2 \Omega\).

Having determined the desired non-Foster impedance \(Z_d(s)\), then \(H(z)\) was designed using the search-based method of Fig. 2 with the three frequencies of error \(E\) being 9.5, 10, and 10.5 MHz in (3). The resulting \(H(z)\) was
\[
H(z) = \frac{12.11z^2 + 2.36z + 1.55}{z^2 + 1.77z + 0.79}
\]

The impedance of the matched antenna is \(Z_{tot}\) shown in Fig. 3 with imaginary part \(\text{Im}(Z_{tot})\) crossing zero near the desired 10 MHz operating frequency, indicating an effective impedance match of the monopole antenna. With \(Z_{tot} = 6.6 - j1.4 \Omega\) at 10 MHz, the real part of \(Z_{tot}\) is 6.6 \(\Omega\), and is denoted \(R_{e}(Z_{tot})\) in Fig. 3. Also shown is the imaginary part of the unmatched antenna \(\text{Im}(Z_{ant})\) and the imaginary part of the digital non-Foster matching network \(\text{Im}(Z_{nonfос})\), where \(\text{Im}(Z_{nonfос}) \approx -\text{Im}(Z_{ant})\) at 10 MHz (The failed design using the earlier method in [4] is shown as \(\text{Im}(Z_{fai})\)). The bandwidth improvement of the digital non-Foster antenna match using the new search-based design is shown in the S-parameters of Fig. 4, for the 5 \(\Omega\) test source shown in Fig. 1. Fig. 4 shows the digital non-Foster match with 6 dB bandwidth of 0.84 MHz, which is more than seven times the 0.11 MHz bandwidth of the passive match.

ACKNOWLEDGMENT

This material is based upon work supported by the National Science Foundation under Grant No. 1731675.

REFERENCES