Copyright 2018 IEEE. Published in 2018 IEEE SoutheastCon, Tampa, FL, 19-22 Apr, 2018. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works, must be obtained from the IEEE, 445 Hoes Lane, Piscataway, NJ 08855, USA. Tel.: 908-562-3966. See https://ieeexplore.ieee.org/search/searchresult.jsp?newsearch=true&queryText=Investigation%20of%20a%20Digital%20Non-

Investigation of a Digital Non-Foster RC Circuit Using Pade and Prony Approximations

Sunny Arokia Swamy Bellary, Nelyadi S. Shetty, Ryan C. Hill, Thomas P. Weldon and James M. Conrad Department of Electrical and Computer Engineering University of North Carolina at Charlotte Charlotte, NC, USA

Email: sbellary@uncc.edu

Abstract—Non-Foster circuits can be used to improve the performance and bandwidth of existing applications, and to enable new technologies such as acoustic cloaking. Although analog approaches for the implementation of non-Foster circuits have existed for some time, digital discrete-time implementations of non-Foster circuits have recently been introduced. Previous digital discrete-time implementations of non-Foster circuits used a backward difference method to design the digital non-Foster circuit. In this paper, Pade and Prony modeling methods are presented for the design of digital non-Foster RC series circuits. The performance of the proposed Pade and Prony methods are compared with the earlier approach using the backward difference method. The Pade and Prony methods were shown to better approximate resistance in the mid bandwidth region than the backward difference method for a positive capacitance and resistance as well as a negative RC circuit. Lastly, a prototype using the Prony method to design a digital positive RC series circuit was implemented on a microcontroller, with measured results closely matching theory.

I. Introduction

Non-Foster circuits can be used to improve performance in a variety of applications, such as impedance matching networks, invisible acoustic sensors, and electrically-small antennas [1]— [6]. Although analog approaches for the implementation of non-Foster circuits have existed for some time, digital discretetime implementation of a non-Foster circuit have only recently been introduced [7].

Prior approaches for the design of digital non-Foster circuits were based on a backward difference method, where a discrete-time backward difference is used to approximate a derivative [7], [8]. This backward difference design method uses an approximation of the differential equations representing the corresponding analog non-Foster circuit to digitally implement the analog circuit. However, other digital discrete-time design techniques may result in alternative designs with different performance characteristics than the earlier backwarddifference method.

non-Foster RC series circuit using Padé and Prony indirect modeling methods [9]. In particular, the performance of the Padé and Prony methods are investigated and compared with the earlier approach using the backward difference method.

Therefore, this paper considers the design of a digital

Section II summarizes the digital non-Foster circuit architecture and prior backward difference design method. In section III and IV, the Padé and Prony approximation methods are described for the design of a digital non-Foster RC series circuit using each method. The theoretical performance of the Padé and Prony methods are compared with the backward difference method in section V. In section VI, measured results are given for a prototype of a Prony-method design of digital positive RC series circuit implemented on a microcontroller.

II. PRIOR BACKWARD DIFFERENCE METHOD

Before discussing the Prony and Padé designs, the theory of digital non-Foster circuits and the prior backward difference design method is reviewed [7], [8]. In Fig. 1, the ADC with clock period T digitizes the analog input voltage signal $v_{in}(t)$ creating a discrete-time signal $v_{in}[n] = v_{in}(nT)$. The DAC input at the output of digital filter H(z) is then

$$v_{DAC}[n] = h[n] * v_{in}[n] \label{eq:vdac}$$

where H(z) in Fig. 1 is the z-transform of impulse response h[n] in the convolution above.

The design goal is to find H(z) that produces the desired analog impedance at $v_{in}(t)$ corresponding to the analog circuit. For the example of the analog RC series circuit shown to

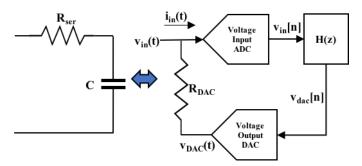


Fig. 1. Block diagram of a digital non-Foster circuit with the corresponding analog circuit shown on the left. The input voltage signal $v_{in}(t)$ is digitized into $v_{in}[n] = v_{in}(nT)$ by the ADC with clock period T. The digitized signal undergoes convolution with the discrete-time filter H(z) resulting in $v_{DAC}[n]$ = $v_{in}[n] * h[n]$. This is converted back into an analog signal $v_{DAC}(t)$ by the DAC. The resistance R_{DAC} , sets the input current $I_{in}(t)$ [7], [8].

the left in Fig. 1, $v_{in}(t)=i_{in}(t)R_{ser}+\frac{1}{C}\int i_{in}(t)dt$. Differentiating with respect to time yields: $\frac{dv_{in}(t)}{dt}=R_{ser}\frac{di_{in}(t)}{dt}+\frac{1}{C}i_{in}(t)$. Applying the backward difference approximation as shown in [7] gives $\frac{dv_{in}(t)}{dt}\approx \frac{v_{in}[n]-v_{in}[n-1]}{T}$ and $i_{in}[n]\approx \frac{v_{in}[n]-v_{DAC}[n-1]}{R_{DAC}}$. This results in the backward difference filter $H_{RC}(\mathbf{z})$ from [8]

$$H_{RC}(z) = \frac{V_{DAC}(z)}{V_{in}(z)}$$

$$= \frac{(R_{ser}C - R_{DAC}C + T)z + (R_{DAC}C + R_{ser}C)}{(R_{ser}C + T)z - (R_{ser}C)}$$
(1)

From [7], the impedance of the non-Foster circuit is

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} \approx \left. \frac{sTR_{DAC}}{sT - H(z)(1 - z^{-1})} \right|_{z = e^{sT}}.$$
 (2)

III. PROPOSED PADÉ DESIGN METHOD

The Padé approximation method is a form of indirect signal modeling [9], where a signal g[n] is directly modeled as the impulse response of a system, where h[n] approximates g[n] and H(z) = Z(h[n]). In the Padé method,

$$H(z) = \frac{Y(z)}{X(z)} = \frac{B(z)}{A(z)}$$

$$= \frac{\sum_{m=0}^{N_B} (b_m z^{-m})}{1 + \sum_{n=1}^{N_A} (b_n z^{-n})} \approx \sum (g[n]z^{-1}) = G(z),$$
(3)

where g[n] is the desired impulse response, X(z) = 1 and $Y(z) \approx G(z)$, then $B(z)X(z) = A(z)Y(z) \approx A(z)G(z)$ results in the Padé approximation form

$$B(z) = A(z)G(z), (4)$$

or, after taking the inverse z-transform:

$$\sum_{k=0}^{N_A} (a[k] g[n-k]) = b[n] \quad where \quad a_0 = 1.$$
 (5)

The Padé method then exactly matches the first few points of h[n] to g[n] by solving for the filter coefficients. In matrix form, the Padé method involves finding the solution for \overline{A} and \overline{B} such that:

$$\overline{\overline{G}} \ \overline{A} = \overline{B} \tag{6}$$

Since, our Padé approximation exactly matches three points then (6) becomes

$$\overline{\overline{G}} \ \overline{A} = \begin{bmatrix} g[0] & 0 \\ g[1] & g[0] \\ g[2] & g[1] \end{bmatrix} \begin{bmatrix} 1 \\ a_1 \end{bmatrix} = \overline{B} = \begin{bmatrix} b_0 \\ b_1 \end{bmatrix}$$
 (7)

where the filter coefficients a_1 , b_0 and b_1 are solved for using Padé procedure given in [9].

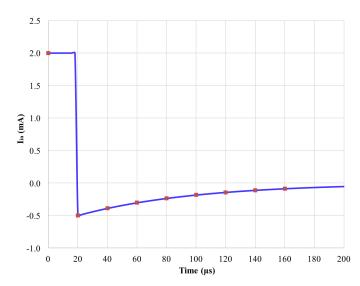


Fig. 2. Current $i_{in}[n]$ for $R_{ser} = 500$ ohms, $C = 0.1 \ \mu\text{F}$, and $T = 20 \ \mu\text{s}$. Blue curve is the continuous-time current $i_{in}(t)$, red dots are discrete-time current samples $i_{in}[n]$.

IV. PROPOSED PRONY DESIGN METHOD

The Prony method forms a solution \overline{A} and \overline{B} given by (6) by minimizing the square error over a variable number of points of g[n], instead of exactly matching the first few points of g[n]. It is based on the method of least squares minimization for an over-determined system in (6). For the first few points, the Prony method has zero error in approximating g[n] by h[n], but typically has error for subsequent points. For an example where eight points of g[n] are used in the Prony method:

$$\overline{\overline{G}} \overline{A} = \begin{bmatrix} g[0] & 0 \\ g[1] & g[0] \\ \vdots & \vdots \\ g[7] & g[6] \end{bmatrix} \begin{bmatrix} 1 \\ a_1 \end{bmatrix} \approx \begin{bmatrix} b_0 \\ b_1 \end{bmatrix} = \overline{B}$$
 (8)

where the filter coefficients a_1 , b_0 and b_1 are solved for using a least-squares Prony procedure given in [9].

V. RESULTS

The three design methods were first evaluated for a digital series RC circuit with an impedance of

$$Z_{inIdeal}(s) = R_{ser} + \frac{1}{sC}$$
 (9)

with R_{ser} equal to 500 ohms, and C equal to 0.1 μ F. The resistor at the DAC output, R_{DAC} , is equal to 1000 ohms for all cases. For the Padé and Prony methods, the impulse response g[n] shown in Fig. 2 was calculated for the capacitor current in an ideal analog positive RC series circuit over an interval of 200 μ s. The red dots in Fig. 2 denote the current samples used for g[n] in the modeling equations (7) and (8) to solve for the Prony and Padé filter coefficients.

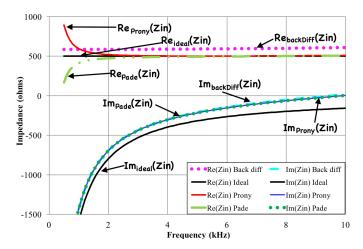


Fig. 3. Comparison of Padé, Prony, and backward difference methods for the positive RC circuit, for resistance $R_{ser}=500$ ohms, C = 0.1 μ F, $R_{DAC}=1000$ ohms, and $T=20~\mu$ s. Real and imaginary parts of Padé, Prony, backward difference models and ideal analog RC circuit impedance are plotted.

For eight current samples used for g[n] in the Prony approximation, the resulting filter is

$$H_{Prony}(z) = \frac{-z + 1.2523}{z - 0.7523}$$
 (10)

Similarly, for three current samples used for g[n] in the Padé approximation, the resulting filter is

$$H_{Pade}(z) = \frac{-z + 1.2788}{z - 0.7788}. (11)$$

Substituting (10) and (11) into (2) yields the theoretical Prony and Padé input impedances plotted in Fig. 3.

The dotted magenta, solid red, dashed green and solid black curves in Fig. 3 denote the real part of the impedance of the backward difference, Prony, Padé and ideal input impedances respectively. The ideal impedance is from (9). Similarly, the dashed cvan, solid blue, dotted green and solid black curves denote the imaginary part of the impedance of the backward difference, Prony, Padé and ideal approximations. The imaginary impedance of the Padé and Prony approximations overlap in Fig. 3, and hence are indistinguishable from each other. Similarly, the real part of the impedance for the Padé and Prony approximations begin to overlap from 2 kHz onward. As seen in Fig. 3, the Padé and Prony designs have larger error in the real part of their impedances at very low frequency, but more nearly equal the desired 500 ohm resistance midband when compared to the backward difference method. The reactance of all three design methods are nearly equal across the entire frequency range.

The design methods were then compared for a digital non-Foster series RC circuit with a $R_{ser}=-500$ ohms and $C=-0.1~\mu\mathrm{F}$. The impulse response g[n] shown in Fig. 4 is created by calculating the capacitor current in an ideal analog negative RC series circuit over a time interval of $200~\mu\mathrm{s}$. The red dots in Fig. 4 denote the current samples used for g[n] in the modeling equations (7) and (8) to solve for the Prony and Padé filter

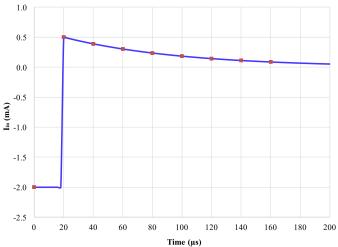


Fig. 4. Current $i_{in}[n]$ for R_{ser} = -500 ohms, C = -0.1 μF and T = 20 μs . Blue curve is continuous-time current, red dots are discrete-time current samples $i_{in}[n]$.

coefficients. The Prony approximation for eight current points is

$$H_{Prony}(z) = \frac{3z - 2.7570}{z - 0.7523} \tag{12}$$

Similarly, the Padé approximation for 3 points is

$$H_{Pade}(z) = \frac{3z - 2.8364}{z - 0.7788} \tag{13}$$

Substituting (12) and (13) into (2) yields the theoretical Prony and Padé input impedances plotted in Fig. 5.

The dotted magenta, solid red, dashed green and solid black curves in Fig. 5 denote the real part of the impedance of the backward difference, Prony, Padé and ideal impedance respectively. Similarly, the dashed cyan, solid blue, dotted green and solid black curves denote the imaginary part of the impedance of the backward difference, Prony, Padé and

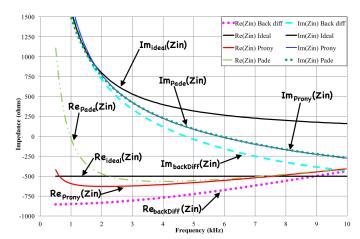


Fig. 5. Comparison of Padé, Prony and backward difference methods for the positive RC circuit, for resistance R= -500 ohms, C = -0.1 μ F, R_{DAC} = 1000 ohms , and T = 20 μ s. Real and imaginary parts of Padé, Prony, backward difference models and ideal analog RC circuit impedance are plotted.

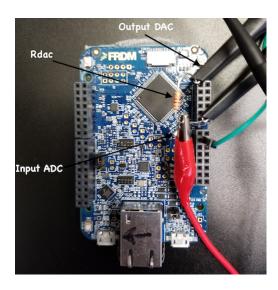


Fig. 6. Prototype using FRDM-K64F microcontroller board.

ideal impedance of (9). As seen in Fig. 5, the Padé and Prony designs have larger error in the real parts of the impedance at very low frequency, but more nearly equal the desired -500 ohms resistance mid-band when compared to the backward difference method. The reactance of the Padé and Prony methods are nearly equal to the ideal reactance across the frequency range.

VI. IMPLEMENTATION

A Freescale FRDM-K64F embedded microcontroller was used to implement the prototype shown in Fig. 6. As proof of concept, a positive digital RC circuit was implemented using the Prony approximation with $R_{ser} = 50$ ohms, $R_{DAC} = 1000$ ohms, $C = 2~\mu F$ and $T = 20~\mu s$. Using (8) for 20 current samples for this design yields a Prony approximation of

$$H_{Prony}(z) = \frac{-19z + 19.5502}{z - 0.8184}.$$
 (14)

Substituting (14) into (2) yields the theoretical Prony input impedances plotted in Fig. 7.

In Fig. 7, the input impedance is plotted for the frequency range 500 Hz to 5 kHz. The dotted magenta, solid red, and dashed black curves show the real part of the impedance of the theoretical Prony, the measured Prony, and the ideal impedance, respectively. Similarly, the solid blue, dashed cyan, and dashed black curves are the imaginary part of the impedance of measured Prony, the theoretical Prony, and the ideal impedance, respectively. As seen in Fig. 7, the theoretical results closely match the measured results for the Prony design.

VII. CONCLUSION

Padé and Prony methods were compared to a previous backward difference method for the design of a digital positive RC and negative RC circuit. The Padé and Prony designs more

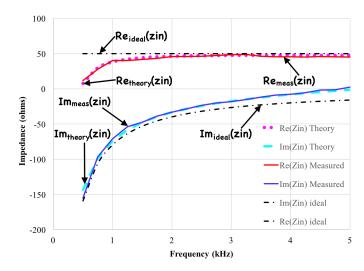


Fig. 7. Comparison of the theoretical, measured, and ideal impedance for $R_{ser}=50$ ohms, $C=2~\mu F$ and $T=20\mu s$. The real and imaginary parts of the theoretical and measured Prony impedance are plotted along with the ideal impedance of the positive RC circuit. The measured impedance closely matches the theoretical Prony impedance calculated from (14).

closely match the desired resistance at the mid-band range, but tended to degrade at very low frequencies compared to the backward difference design. The reactance of the Padé and Prony designs closely matched the backward difference design for the positive RC circuit. However, the reactance of the Padé and Prony designs for the negative RC circuit more closely match the ideal impedance when compared to the backward difference design. Measured impedance of a prototype Prony design closely matches the predicted theoretical impedance.

REFERENCES

- N. Zhu and R. W. Ziolkowski, "Active metamaterial-inspired broadbandwidth, efficient, electrically small antennas," *IEEE Antennas and Wireless Propagation Letters*, vol. 10, pp. 1582–1585, 2011.
- [2] Keum-Su Song and R. G. Rojas, "Non-Foster impedance matching of electrically small antennas," in 2010 IEEE Antennas and Propagation Society International Symposium, Jul 2010, pp. 1–4.
- [3] R. Fleury, D. Sounas, and A. Alù, "An invisible acoustic sensor based on parity-time symmetry," *Nature Communications*, vol. 6:5905, pp. 1–7, Jan. 2015.
- [4] S. D. Stearns, "Incorrect stability criteria for non-Foster circuits," in Proceedings of the 2012 IEEE International Symposium on Antennas and Propagation. IEEE, Jul 2012, pp. 1–2.
- [5] M. Jacob, J. Long, and D. F. Sievenpiper, "Broadband non-Foster matching of an electrically small loop antenna," in 2012 IEEE Antennas and Propag. Soc. Int. Symp. (APSURSI), Jul. 2012, pp. 1–2.
- [6] S. E. Sussman-Fort and R. M. Rudish, "Non-Foster impedance matching of electrically-small antennas," vol. 57, no. 8, pp. 2230–2241, Aug. 2009.
- [7] T. P. Weldon, J. M. C. Covington, K. L. Smith, and R. S. Adams, "Performance of digital discrete-time implementations of non-Foster circuit elements," in 2015 IEEE International Symposium on Circuits and Systems (ISCAS), May 2015, pp. 2169–2172.
- [8] P. J. Kehoe, K. K. Steer, and T. P. Weldon, "Thevenin forms of digital discrete time non-Foster RC and RL circuits," in 2016 IEEE International Symposium on Antennas and Propagation (APSURSI), Jun 2016, pp. 191– 192.
- [9] M. H. Hayes, Statistical Digital Signal Processing and Modeling, 1st ed. John Wiley and Sons, Inc, 1996.