Experimental Results for an Inductively Matched Microwave Amplifier in a Standard 0.5 Micron CMOS Process Using Four Identical Spiral Inductors

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Abstract

Experimental results are presented for an inductively-matched microwave amplifier design in a standard 0.5 micron CMOS process. For the amplifier design, inductive source degeneration is used to provide input impedance matching with on-chip planar spiral inductors. In the proposed approach, four identical spiral inductors are used in the circuit to reduce design complexity for use in course projects. The use of identical spiral inductors also allows the fabricated devices to be characterized by simple parametric measurement of a single spiral inductor. Input return loss for a prototype amplifier was measured to be better than 10 dB from 1.0 to 1.8 GHz. Even with limited gain, the prototype effectively illustrates the proposed design approach. Measurements of the impedance of the on-chip spiral inductor are also provided.

1. Introduction

On-chip spiral inductors play an important role in extending the frequency range of commercial CMOS (complementary metal-oxide semiconductor) processes [1]. In particular, the inductive source degeneration method can be used to support the design of microwave and radio frequency amplifiers in CMOS processes [2]-[3]. In this method, inductors are placed in series with the gate and source of an MOS (metal oxide semiconductor) transistor to match the input impedance of an amplifier design. Although it may be desirable to incorporate an example of this design method into a laboratory course, the non-trivial design of the requisite spiral inductors could limit the fabrication success rate of course projects.

To mitigate some of the complexity of an inductive source degeneration amplifier design, a simplified design is proposed. In particular, four identical spiral inductors are used in the circuit to reduce design complexity for use in course projects. Three inductors are used in series with the gate of the MOS transistor, and one inductor is used in series with the source of the MOS transistor. Thus, a single spiral inductor design is required. Replication of a single spiral inductor design reduces potential for integrated circuit layout errors. In addition, all of the inductors in the circuit can then be characterized by measuring a single spiral inductor after fabrication. Furthermore, the spiral inductor design may be reused in subsequent courses, and simulation accuracy can be enhanced by using measured data from previous fabrication runs.

In the following, a four-inductor amplifier design, spiral inductor, and simulation results are first presented. Following this, measured data is given for a fabricated amplifier and shown to correspond well with calculated results and simulation results.

2. Design and Simulation

The schematic of the proposed four-inductor amplifier design is shown in Fig. 1. As previously noted, the design is intended for a standard CMOS process, and in the schematic a NMOS (n-channel metal oxide semiconductor) transistor is chosen. The input port P_{in} is connected to the gate of the transistor through three identical inductors. The source of the transistor is connected to ground through a single inductor. Finally, the output port P_{out} is connected to the drain. In Fig. 1, dc bias is provided externally to the two ports P_{in} and P_{out} using bias tees.

The circuit configuration of Fig. 1 is a typical inductive source degeneration topology, except that the input inductor is split into three inductors that are identical to the source inductor. Thus, only one spiral inductor must be designed for circuit layout. As noted earlier, this reduces the potential for layout error in course projects, since the spiral inductor design can be easily replicated in layout. In addition, the circuit simplifies the characterization of fabricated devices, since only the measurement of a single spiral inductor characterizes all inductors used in the circuit.

Each of the spiral inductors in Fig. 1 was implemented with the layout shown in Fig. 2. The outer dimensions of the spiral are 190×190 microns, and the inner area without metal was 70×70 microns. The spiral arms were 12 microns in width, using top-metal for minimal series resistance and minimal stray capacitance.

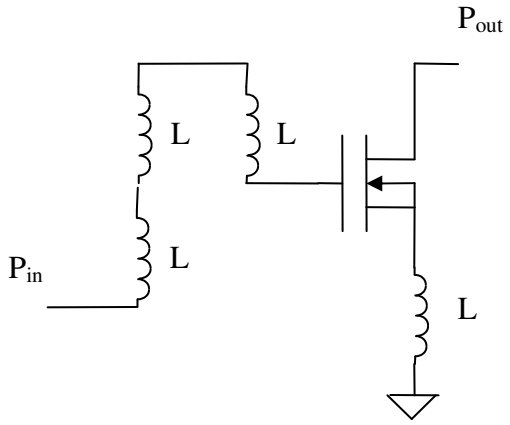

Figure 1. CMOS amplifier design using an NMOS transistor and four identical inductors.

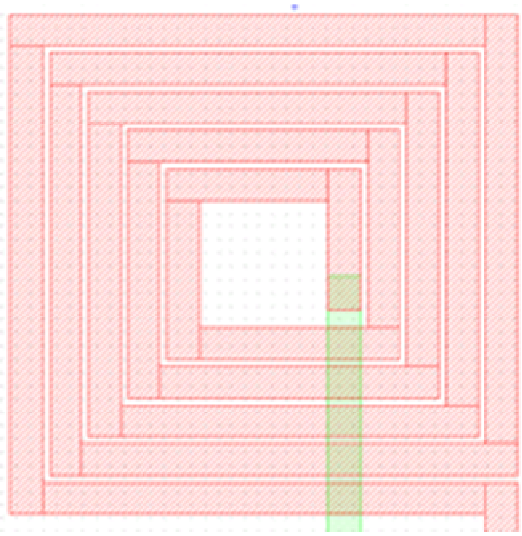

Figure 2. Spiral inductor layout, 5 turns, approx 190×190 micron outer size, 70×70 micron center, 12 micron wide top-metal.

Although a variety of methods are available for modeling spiral inductors, the design of Fig. 2 was based on measurements of devices from other fabrication runs. Measured data for the inductor of Fig. 2 is provided in the Smith chart of Fig. 3. The spiral had a measured inductance of 3.5 nH with losses corresponding to an effective series resistance of 14 ohm at 1 GHz.

The impedance, $Z_g(\omega)$, looking into the gate of the transistor of Fig. 1 is approximated as [3]:

$$Z_g(\omega) \approx \frac{1}{j\omega C_{gs}} + j\omega L + g_m \frac{L}{C_{gs}} \quad , \qquad (1)$$

where L is the inductance of a single inductor, and where g_m and C_{gs} are the conductance and gate-source capacitance of the NMOS transistor. Next, adding the effect of the series resistance of the inductor, R_s, the impedance at the gate becomes

$$Z_g(\omega) \approx \frac{1+g_m R_s}{j\omega C_{gs}} + j\omega L + R_s + g_m \frac{L}{C_{gs}} \quad . \quad (2)$$

For the circuit of Fig. 1, C_{gs}=0.9 pf, L=3.5 nH, Rs = 14 Ω, and g_m = 0.084 S. Using these values, the calculated gate impedance is Z_g =340 – j360. However, this impedance is further reduced by the Miller capacitance associated with the gate-drain capacitance C_{gd}. To find the Miller capacitance, the gate-drain voltage gain $A_{gd}(\omega)$ approximated as

$$A_{gd}(\omega) \approx \frac{-g_m R_L}{1+(g_m+j\omega C_{gs})(R_s+j\omega L)} \quad , \qquad (3)$$

where R_L is the load resistance at the output of Fig. 1. Then, the Miller capacitance is $C_m=C_{gd}(1-A_{gd}(\omega))$. For R_L=50, $A_{gd}(\omega)$=1.5, and C_{gd}=0.23 pF, then C_m=0.6 pF at 1 GHz. The total input impedance at the gate is then the Miller impedance in parallel with the gate impedance, $(1/j\omega C_m)||Z_g(\omega)$ which equals 32 – j184 Ω. Finally, the total input impedance, $Z_{in}(\omega)$, as seen at the input of Fig. 1 is

$$Z_{in}(\omega) \approx 3j\omega L + 3R_s + \frac{Z_g(\omega)}{1+j\omega C_m Z_g(\omega)} \quad . \qquad (4)$$

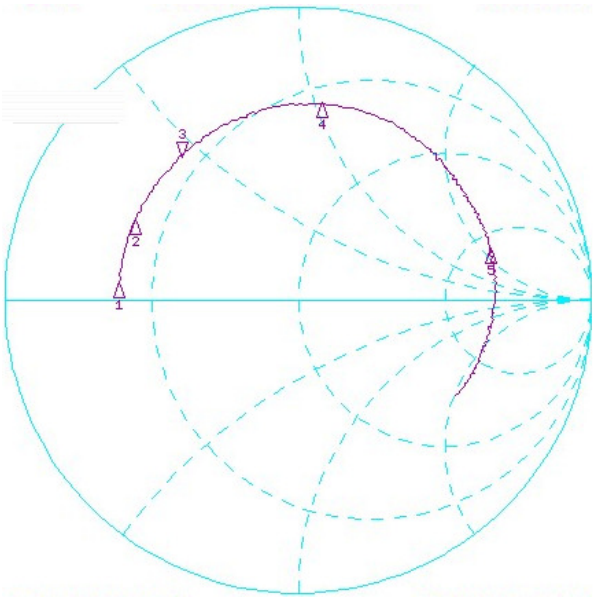

Figure 3. Measured results for spiral inductor of Fig. 2, with impedance of 14 + j23 ohms, equivalent to 3.5 nH at 1.0 GHz (marker 3).

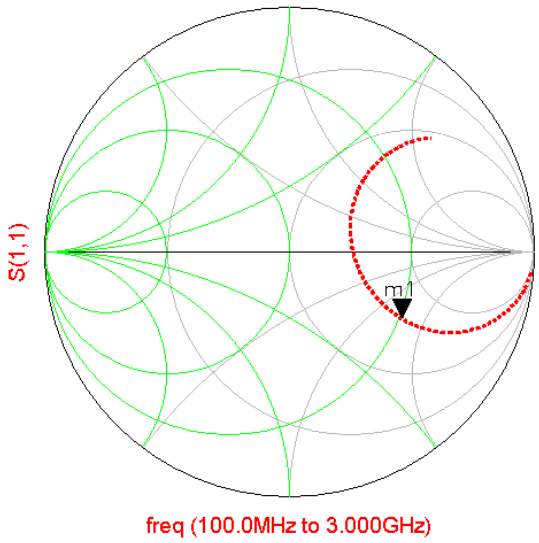

Figure 4. Simulation results showing S_{11} (dashed red curve) for design of Fig. 1. Impedance at 1 GHz (marker 1) is 98 – j75 Ω.

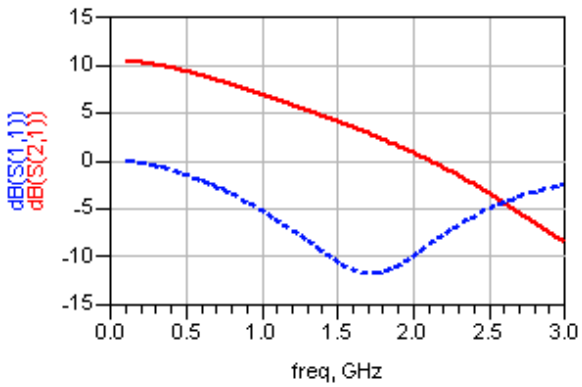

Figure 5. Simulation results showing $|S_{11}|$ (dashed blue curve) and $|S_{21}|$ (solid red curve) for design of Fig. 1. Gain is 6.8 dB at 1 GHz.

Using Eq. (4), the calculated input impedance at 1 GHz is then $Z_{in}(\omega) = 74 - j118\ \Omega$.

The circuit of Fig. 1 was also simulated for the inductor of Fig. 2 and with a BSIM3 model for the 1000×0.5 NMOS transistor in the AMI Semiconductor 0.5 micron CMOS process. The input gate dc bias was 1 volt and the output drain dc bias was 3.3 volts. The S_{11} s-parameter simulation results of Fig. 4 show a predicted input impedance of 98 – j75 Ω at 1 GHz. The simulated value is not in exact agreement with the calculated value, due to simplifying approximations used in Eq. (4).

The s-parameter simulation results of Fig. 5 show the magnitude of predicted S_{11} and S_{21}. The inductive source degeneration exhibits the best return loss near 1.5 GHz, as evidenced by the minimum of S_{11} in Fig. 5. In particular, the return loss at the input port is better than 10 dB from 1.4 GHz to 2.0 GHz. The simulated gain (S_{21}) is approximately 6.8 dB at 1 GHz and 4 dB at 1.5GHz. The gain level was somewhat lower than the design target because of the losses associated with the modest Q of the chosen spiral inductor design.

Despite the modest gain in Fig. 5, the effects of inductive source degeneration are clearly evident in the "dip" in the plot of S_{11}. Similarly, the effect of inductive source degeneration can be seen in the Smith chart of Fig. 4, where the inductive reactance causes the input impedance to move from the capacitive region (lower half) to the inductive region (upper half) of the Smith chart. Therefore, the circuit of Fig. 1 suffices to demonstrate the proposed approach using four identical inductors to implement inductive source degeneration for input impedance matching in CMOS. Other variations are possible using different spiral inductor designs, transistor geometries, and device bias levels.

A photograph of the fabricated design is shown in Fig. 6. In this figure, the four spiral inductor designs are clearly visible. The three spirals at the top of Fig. 6 correspond to the three input inductors in the schematic of Fig. 1. The lower spiral of Fig. 6 corresponds to the source inductor of Fig. 1.

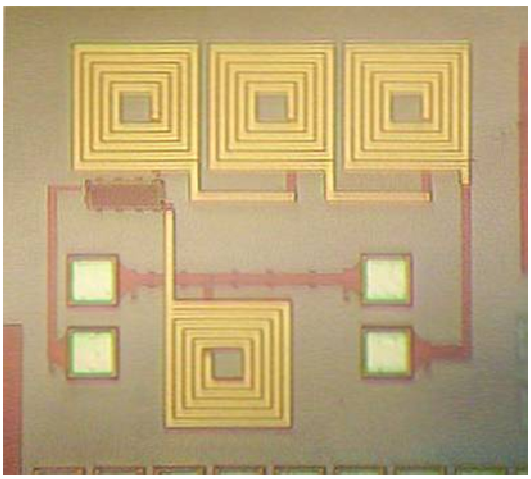

Figure 6. Photograph of chip showing three input spiral inductors at top, source spiral inductor at bottom.

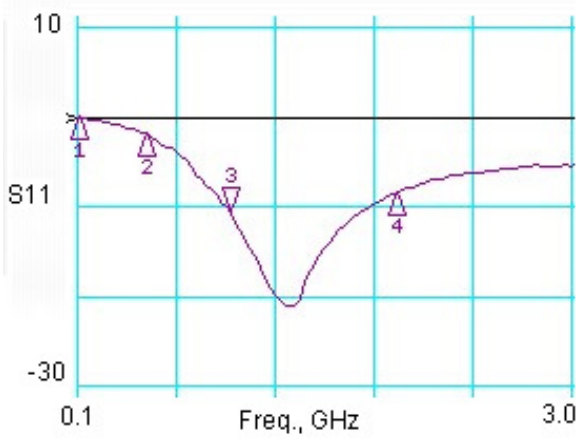

Figure 7. Measured results showing $|S_{11}|$ for design of Fig. 1. Horizontal axis is frequency from 100 MHz to 3 GHz, vertical axis is S_{11} from -30 to +10 dB. Marker 3 shows S_{11} of -10 dB at 1 GHz, marker 4 shows S_{11} of -8.5 dB at 2 GHz.

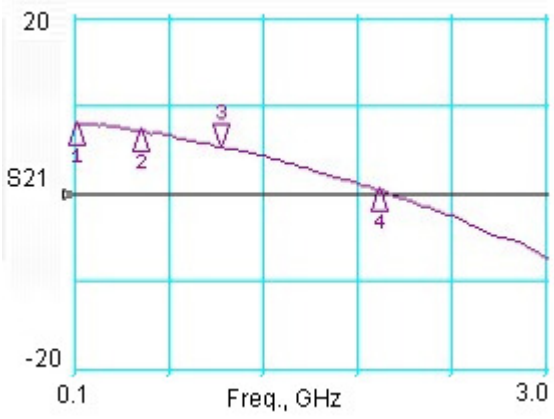

Figure 8. Measured results showing $|S_{21}|$ for design of Fig. 1. Horizontal axis is frequency from 100 MHz to 3 GHz, vertical axis is S_{21} from -20 to +20 dB. Marker 3 shows S_{21} of 5.4 dB at 1 GHz, Marker 4 shows S_{21} of 0 dB at 2 GHz.

3. Measured Experimental Results

The amplifier of Fig. 1 was fabricated in the AMI 0.5 micron CMOS process using the MOSIS chip fabrication service [5]. Measurements were performed with 1.0 V dc input bias to the gate of Fig. 1, and 3.3 V dc output bias at the drain. Under these conditions, a drain current of 10 mA was measured. The measured input impedance, $|S_{11}|$, of the amplifier is shown in Fig. 7. The effect of inductive source degeneration is evident where the return loss dips to a minimum near 1 GHz. The measured return loss is better than 10 dB from 1 GHz to 1.8 GHz. By comparison, the simulated results of Fig. 5 show return loss better than 10 dB from 1.4 GHz to 2.0 GHz.

The measured gain of the amplifier, $|S_{21}|$, is shown in Fig. 8. The measured gain of 5.4 dB at 1 GHz is modestly lower than the simulated gain of 6.8 dB in Fig. 5. In the measured gain of Fig. 8 and simulated gain of Fig. 5, the inductive source degeneration causes no observable resonance in the $|S_{21}|$ frequency response. Although not a focus of the present discussion, the noise figure was measured to be 6.5 dB at 1 GHz. By comparison, a competing resistive feedback design measured 5 dB noise figure, but it consumed significantly more current.

Finally, measurement of the input impedance S_{11} is shown in Fig. 9 on a Smith chart, with marker 3 indicating a frequency of 1 GHz. As in the simulation, the inductive reactance causes the input impedance to move from the capacitive region (lower half) to the inductive region (upper half) of the Smith chart. The measured input impedance at 1 GHz was 46 – j31 Ω, at the location of the marker in Fig. 9. This measured input impedance corresponds well with the calculated value of $Z_{in}(\omega) = 74 - j118\ \Omega$ from Eq. (4), and the simulated value of 98 – j75 Ω. Some discrepancy was expected due to the approximations used and radio frequency limitations of BSIM3 models [5].

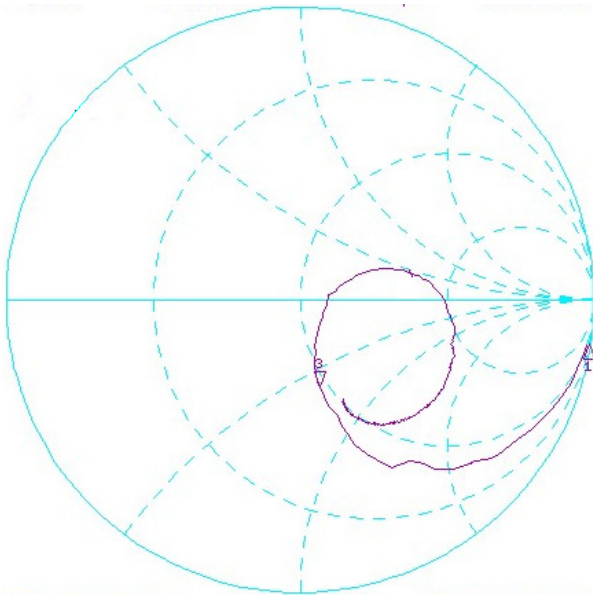

Figure 9. Measured results showing S_{11} for design of Fig. 1. Marker 3 at 1 GHz shows an input impedance of 46 – j31 Ω.

4. Conclusion

An inductively-matched microwave amplifier design was presented, using four identical spiral inductors. The input matching network is comprised of three identical inductors in series with the gate, and a fourth inductor in series with the source of an NMOS transistor. Experimental results for a prototype amplifier confirm the efficacy of the proposed design approach, with measured input return loss better than 10 dB from 1.0 to 1.8 Ghz.

5. Acknowledgements

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6. References

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