Effect of External Source Impedance on the Input Impedance of Digital Impedance Circuits

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***Abstract*—The input impedance of recently-introduced digital impedance circuits has been discovered to be dependent on the impedance of the external signal source. To address this problem, the theory for the dependence of digital impedance on external source resistance is presented. These digital impedance circuits provide an important digitally-controlled digitally-tunable alternative approach to difficult design problems, such as design of negative capacitances for stable wideband non-Foster antennas and metamaterials. Unfortunately, undesired source-dependent variation of the digital impedance can arise in scenarios where off-the-shelf high-speed analog-to-digital and digital-to-analog converters commonly have 50 ohm impedance. Further complicating matters, the sensitivity of digital impedance on source resistance appears to also depend on other design parameters of the digital circuit. Therefore, theory and simulation results are presented to show the dependence of digital impedance on the external source resistance. Lastly, measured results for a prototype of a digital non-Foster negative capacitance confirm the theoretical results.**

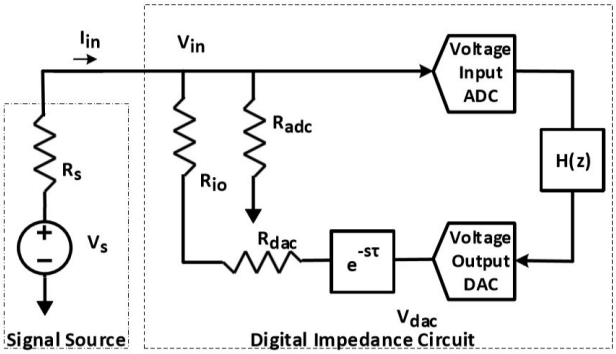

Fig. 1. Block diagram of a digital impedance circuit driven by an external voltage source $V_s(s)$ and a source resistor R_s. The desired digital input impedance $Z_{in}(s) = V_{in}(s)/I_{in}(s)$ is established by designing the digital transfer function $H(z)$ for given values of R_s, R_{adc}, R_{dac}, and R_{io}.

I. Introduction

Digital impedance circuits offer an alternative approach for the design of difficult-to-stabilize negative capacitances and negative inductances for use in challenging applications such as wideband impedance matching in metamaterials and electrically-small antennas [1]–[5]. Early implementations of such digital impedance circuits utilized ideal current-source DACs (digital-to-analog converters) or ideal ADCs (analog-to-digital converters) with infinite input impedance [6]. However, practical off-the-shelf high-frequency ADCs and DACs commonly have low impedances of 50 ohms, requiring more complicated digital designs for digital impedance circuits to achieve impedances much greater than the impedance of the ADCs and DACs in the system [4]. Unexpectedly, it was also discovered that the input impedance of these digital impedance circuits was affected by the impedance of the external signal source. Further complicating matters, the variation of digital circuit impedance was observed to occur over a limited range of external source impedance. Thus, more recent investigations with 50-ohm converters seems to have uncovered important phenomena that must be included in a new extension of earlier analysis and theory.

To address the issue of unexpected digital impedance variation as a function of source resistance, detailed analysis and theory is provided showing this unexpected dependence. (In the following, "digital impedance" refers to the input impedance of a digital impedance circuit.) While the underlying system equations and analysis are relatively straightforward, the analytic solution showing the dependence on source resistance is shown to be extraordinarily complicated. Nevertheless, simulation and experimental results are used to confirm the theory for a few example designs.

In the following section, the theoretical effect of source resistance on digital impedance is derived. The next section discusses simulation results in comparison to the theory for two example systems with digital impedance designs for an open circuit and for a negative capacitance. The following section presents the measured results for a microcontroller-based prototype of a digital negative capacitance.

II. Theory

A block diagram of the digital impedance circuit is provided on the right of Fig. 1. The digital impedance circuit input current and voltage are represented as I_{in} and V_{in} respectively. The digital impedance circuit is driven by an external voltage source with source resistance R_s. Resistors R_{adc} and R_{dac} are the input resistance of the ADC and the output resistance of the DAC respectively, and R_{io} is a resistor coupling between the DAC output and ADC input. The ADC digitizes V_{in}, and the DAC output is V_{dac}. The z-transform transfer function $H(z)$ represents the digital signal processing required to synthesize the desired digital impedance $Z_{in}(s) = V_{in}(s)/I_{in}(s)$ in the Laplace domain [4], [6]. Here, $H(z)$ is an arbitrary discrete

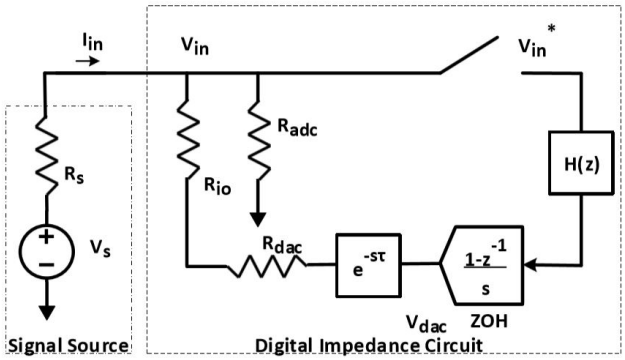

Fig. 2. Analysis block diagram of a digital impedance circuit driven by an external voltage source $V_s(s)$ and a source resistor R_s. The ADC of Fig. 1 is modeled by the ideal sampler, and the voltage after the sampler is the starred transform $V_{in}^{\star}(s)$ of the input voltage $V_{in}^{\star}(s)$. The ZOH (zero-order hold) transfer function $(1-z^{-1})/s$ models the DAC output V_{dac}.

transfer function which can be designed to implement the desired impedance $Z_{in}(s)$. The time delay block $e^{-s\tau}$ in Fig. 1 accounts for the latency of the signal-processing computation time, along with the ADC and DAC conversion times.

The full analysis of the system in Fig. 1 is considered next, to demonstrate that the digital input impedance $Z_{in}(s)$ is affected by the source impedance R_s. First, the system of Fig. 1 is analyzed using the block diagram of Fig. 2, where $V_{in}^{\star}(s)$ is the starred transform of V_{in} [7], and $V_s(s)$ is the source voltage. The ADC of Fig. 1 is replaced by the ideal sampler in Fig. 2, with the sampler output $V_{in}^{\star}(s)$ being the starred transform of the input voltage $V_{in}(s)$. The DAC output is formed by passing through the ZOH (zero-order hold) with transfer function $(1-z^{-1})/s$. The ZOH output in Fig. 2 passes through the same delay as in Fig. 1.

The input voltage from Fig. 2 in the Laplace domain is given as:

$$V_{in}(s) = \left. \frac{\frac{V_s(s)}{Rs} + \frac{V_{in}^{\star}(s)e^{-s\tau}H(z)(1-z^{-1})/s}{R_{io}+R_{dac}}}{\frac{1}{R_s}+\frac{1}{R_{adc}}+\frac{1}{R_{io}+R_{dac}}} \right|_{z=e^{sT}}, \quad (1)$$

where T is the sampling period of the ADC and DAC. To find $V_{in}^{\star}(s)$, we take the starred transform of both sides of (1) as follows:

$$\begin{aligned} V_{in}^{\star}(s) &= \left. \frac{\frac{V_s^{\star}(s)}{Rs} + \frac{V_{in}^{\star}(s)H(z)z^{-1}}{R_{io}+R_{dac}}}{\frac{1}{R_s}+\frac{1}{R_{adc}}+\frac{1}{R_{io}+R_{dac}}} \right|_{z=e^{sT}} \\ &\approx \left. \frac{\frac{V_s(s)}{RsT} + \frac{V_{in}^{\star}(s)H(z)z^{-1}}{R_{io}+R_{dac}}}{\frac{1}{R_s}+\frac{1}{R_{adc}}+\frac{1}{R_{io}+R_{dac}}} \right|_{z=e^{sT}}, \end{aligned} \quad (2)$$

for frequencies below $1/(2T)$, where $V_s^{\star}(s) \approx V_s(s)/T$ for bandlimited $V_s(s)$ without aliasing. The starred transform of $V_{in}^{\star}(s)e^{-s\tau}H(z)(1-z^{-1})/s$ follows from the modified z-transform of $e^{-s\tau}(1-z^{-1})/s$ becoming z^{-1} [7].

The input current is found by the voltage difference between the source V_s and the input V_{in}, divided by the source resistance:

$$I_{in}(s) = \frac{V_s(s) - V_{in}(s)}{R_s}. \quad (3)$$

Despite the relative simplicity of the foregoing equations, the solution for the digital impedance $Z_{in}(s)$ is extraordinarily complicated. Using a commercial symbolic solver, the digital input impedance is found to be:

$$\begin{aligned} Z_{in}(s) \;=\; & (H(z)\,R_{adc}^2\,R_{dac}\,R_s\,z \;-\; H(z)\,R_{adc}^2\,R_{io}\,R_s \;- \\ & H(z)\,R_{adc}^2\,R_{dac}\,R_s \;+\; H(z)\,R_{adc}^2\,R_{io}\,R_s\,z \;+ \\ & R_{adc}^2\,R_{dac}^2\,s\,T\,z\,e^{s\tau} \;+\; R_{adc}^2\,R_{io}^2\,s\,T\,z\,e^{s\tau} \;- \\ & H(z)\,R_{adc}^2\,R_{dac}\,R_s\,s\,T\,e^{s\tau} \;-\; H(z)\,R_{adc}^2\,R_{io}\,R_s\,s\,T\,e^{s\tau} \;+ \\ & 2\,R_{adc}^2\,R_{dac}\,R_{io}\,s\,T\,z\,e^{s\tau} \;+\; R_{adc}\,R_{dac}^2\,R_s\,s\,T\,z\,e^{s\tau} \;+ \\ & R_{adc}^2\,R_{dac}\,R_s\,s\,T\,z\,e^{s\tau} \;+\; R_{adc}\,R_{io}^2\,R_s\,s\,T\,z\,e^{s\tau} \;+ \\ & R_{adc}^2\,R_{io}\,R_s\,s\,T\,z\,e^{s\tau} + 2\,R_{adc}\,R_{dac}\,R_{io}\,R_s\,s\,T\,z\,e^{s\tau}) \\ & \div \\ & (H(z)\,R_{adc}^2\,R_{dac} \;+\; H(z)\,R_{adc}^2\,R_{io} \;-\; H(z)\,R_{adc}^2\,R_{dac}\,z \;- \\ & H(z)\,R_{adc}^2\,R_{io}\,z - H(z)\,R_{adc}^2\,R_s\,s\,T\,e^{s\tau} + R_{adc}\,R_{dac}^2\,s\,T\,z\,e^{s\tau} + \\ & R_{adc}^2\,R_{dac}\,s\,T\,z\,e^{s\tau} + R_{adc}\,R_{io}^2\,s\,T\,z\,e^{s\tau} + R_{adc}^2\,R_{io}\,s\,T\,z\,e^{s\tau} + \\ & R_{adc}^2\,R_s\,s\,T\,z\,e^{s\tau} \;+\; R_{dac}^2\,R_s\,s\,T\,z\,e^{s\tau} \;+\; R_{io}^2\,R_s\,s\,T\,z\,e^{s\tau} \;- \\ & H(z)\,R_{adc}\,R_{dac}\,R_s\,s\,T\,e^{s\tau} \;-\; H(z)\,R_{adc}\,R_{io}\,R_s\,s\,T\,e^{s\tau} \;+ \\ & 2\,R_{adc}\,R_{dac}\,R_{io}\,s\,T\,z\,e^{s\tau} \;+\; 2\,R_{adc}\,R_{dac}\,R_s\,s\,T\,z\,e^{s\tau} \;+ \\ & 2\,R_{adc}\,R_{io}\,R_s\,s\,T\,z\,e^{s\tau} + 2\,R_{dac}\,R_{io}\,R_s\,s\,T\,z\,e^{s\tau})\;|_{z=e^{sT}}\,. \end{aligned} \quad (4)$$

Since R_s appears on the right side of (4), the digital impedance $Z_{in}(s)$ is shown to depend on source resistance R_s.

III. Simulation

The Simulink schematic of Fig. 3 was utilized to simulate the system of Fig. 1. The simulation was done with ADC and DAC sampling rates of 100 MHz, with a latency of $\tau = 1$ ns, and with resistors $R_{adc} = 50\,\Omega$, $R_{dac} = 50\,\Omega$, and $R_{io} = 50\,\Omega$ in Fig. 3. The discrete transfer function was set to $H(z) = 3$ (resulting in $Z_{in}(s)$ approximating an open circuit at low frequency).

To demonstrate the dependence of $Z_{in}(s)$ on source resistance R_s, the system of Fig. 3 was simulated with source resistance values of 1 Ω and 1000 Ω. The solid red and dashed magenta lines in Fig. 4 correspond to the Simulink simulation results for the real part $\mathrm{Re}\{Z_{in}(s)\}$ for $R_s = 1\ \Omega$ and $R_s = 1000\ \Omega$ respectively. The solid blue and dashed cyan lines correspond to the simulation results for the imaginary part $\mathrm{Im}\{Z_{in}(s)\}$ for $R_s = 1\ \Omega$ and $R_s = 1000\ \Omega$ respectively. The overlaid circles are the theoretical response computed from (4) for $R_s = 1\ \Omega$, and the overlaid $\times$'s are the theoretical response from (4) for $R_s = 1000\ \Omega$. The theoretical and simulated output at 10 MHz for $R_s = 1\,\Omega$ is approximately $Z_{in}(s) = 21 - j86$, and for $R_s = 1000\,\Omega$ is approximately $Z_{in}(s) = 30 - j54$. Consequently, the digital input impedance $Z_{in}(s)$ changes considerably as the source resistance R_s varies. Note that the behavior at higher frequencies in Fig. 4 resembles that of a capacitor, where this capacitive behavior is induced by the phase lag due to non-zero latency and ZOH phase response.

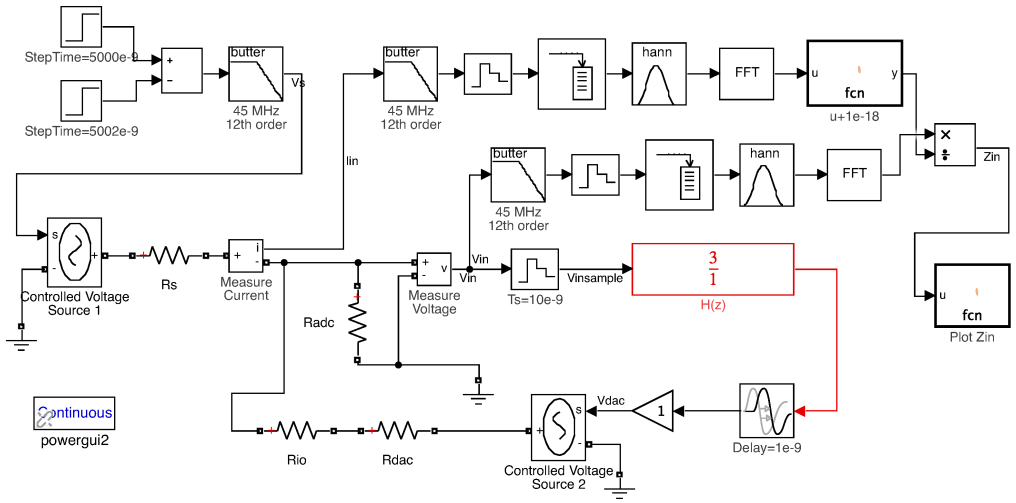

Fig. 3. Simulink simulation schematic for $H(z) = 3$, with R_s, R_{adc}, R_{dac}, and R_{io} shown. Sample time is $T = 10$ ns, and latency is $\tau = 1$ ns. Input is a 45 MHz lowpass-filtered 2 ns wide pulse. The FFT of V_{in} divided by the FFT of I_{in} is used to compute digital input impedance $Z_{in}(s)$.

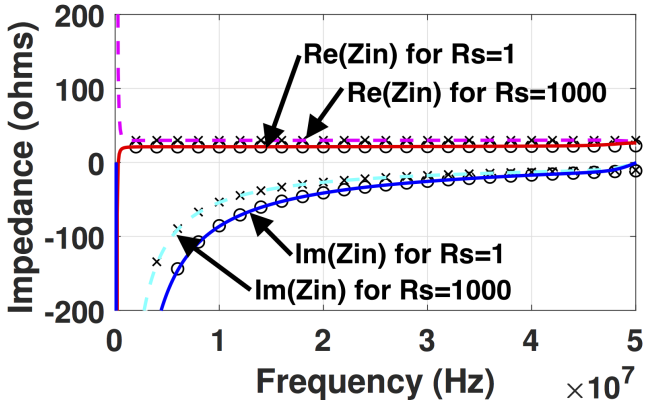

Fig. 4. Theoretical and simulated digital input impedance $Z_{in}(s)$ as a function of frequency for $H_z(z) = 3$, $R_{adc} = 50\,\Omega$, $R_{dac} = 50\,\Omega$, and $R_{io} = 50\,\Omega$. Sample time is $T = 10$ ns, and latency is $\tau = 1$ ns. Solid curves are Simulink simulation results for source impedance $R_s = 1\,\Omega$ with measured $\mathrm{Re}\{Z_{in}\}$ in red and $\mathrm{Im}\{Z_{in}\}$ in blue, with overlaid circles showing theoretical values. Dashed curves are simulation results for source impedance $R_s = 1000\,\Omega$ with measured $\mathrm{Re}\{Z_{in}\}$ in dashed magenta, measured $\mathrm{Im}\{Z_{in}\}$ in dashed cyan, with $\times$'s showing theoretical values.

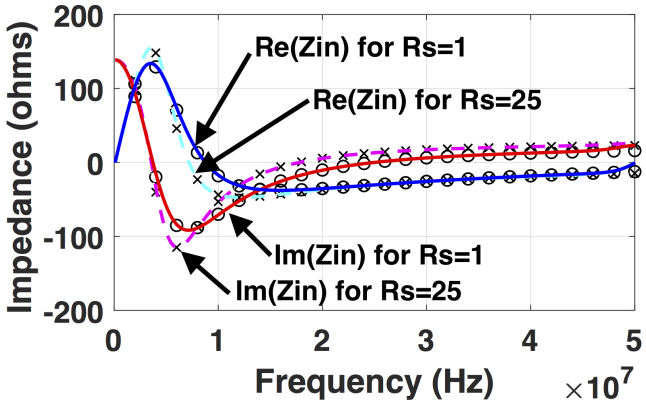

Fig. 5. Theoretical and simulated digital input impedance $Z_{in}(s)$ as a function of frequency for $H_z(z) \approx (4.62z{-}3.78)/(z{-}0.63)$, $R_{adc} = 50\,\Omega$, $R_{dac} = 50\,\Omega$, and $R_{io} = 50\,\Omega$. Sample time is $T = 10$ ns, and latency is $\tau = 1$ ns. Solid curves are Simulink simulation results for source impedance $R_s = 1\,\Omega$ with measured $\mathrm{Re}\{Z_{in}\}$ in red and $\mathrm{Im}\{Z_{in}\}$ in blue, with circles showing theoretical values. Dashed curves are simulation results for source impedance $R_s = 25\,\Omega$ with measured $\mathrm{Re}\{Z_{in}\}$ in dashed magenta, measured $\mathrm{Im}\{Z_{in}\}$ in dashed cyan, with $\times$'s showing theoretical values.

As a second example, a digital negative capacitance was designed for operation near 5 MHz and simulated by setting the discrete transfer function of Fig. 3 to $H_z \approx (4.62z - 3.78)/(z - 0.63)$. This simulation was done with ADC and DAC sampling rates of 100 MHz, a latency delay of 1 ns, and with resistors $R_{adc} = R_{dac} = R_{io} = 50\,\Omega$. To demonstrate dependence of $Z_{in}(s)$ on source impedance R_s, two values of $R_s = 1\ \Omega$ and $R_s = 25\ \Omega$ were simulated. Fig. 5 shows the simulation results, where the reactance between approximately 5 MHz and 10 MHz demonstrates the non-Foster behavior of negative capacitance [8].

The solid red and dashed magenta lines in Fig. 5 correspond to the Simulink simulation results for the real part $\mathrm{Re}\{Z_{in}(s)\}$ for $R_s = 1\ \Omega$ and $R_s = 25\ \Omega$ respectively. The solid blue and dashed cyan lines correspond to the simulation results for the imaginary part $\mathrm{Im}\{Z_{in}(s)\}$ for $R_s = 1\ \Omega$ and $R_s = 25\ \Omega$ respectively. The overlaid circles are the theoretical response computed from (4) for $R_s = 1\ \Omega$, the overlaid $\times$'s are the theoretical response from (4) for $R_s = 25\ \Omega$. The theoretical and simulated output at 5 MHz for $R_s = 1\,\Omega$ is approximately $Z_{in}(s) = -61 + j105$, and for $R_s = 25\,\Omega$ is approximately $Z_{in}(s) = -97 + j105$. Thus, the digital input impedance $Z_{in}(s)$ changes when source resistance R_s changes, as predicted in (4).

IV. Prototype and Measured Data

In our experiments we have observed that sensitivity to source impedance, R_s, is not prevalent in all regions of pa-

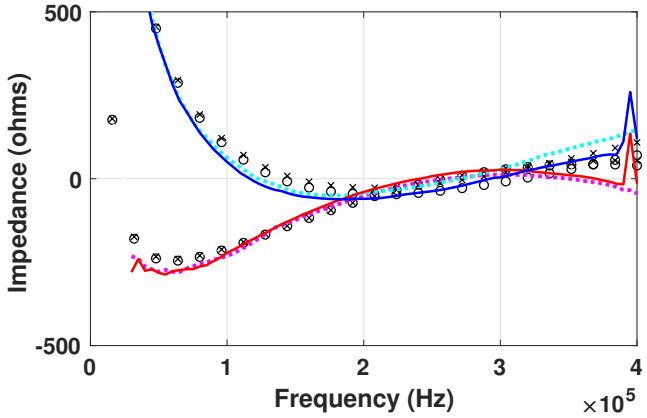

Fig. 6. Prototype measured digital input impedance $Z_{in}(s)$ as a function of frequency for a $H(z) = (22z - 19)/(2z + 1)$ digital design for -8.25 nF negative capacitor in series with 50 ohms resistance. $R_{adc} = 4700\,\Omega$, $R_{dac} = 1\,\Omega$, and $R_{io} = 1000\,\Omega$. Sample time was measured to be $T = 1250$ ns, and latency was measured to be $\tau = 925$ ns. Solid curves are measured results for source impedance $R_s = 50\,\Omega$ with measured $\mathrm{Re}\{Z_{in}\}$ in red and $\mathrm{Im}\{Z_{in}\}$ in blue, with circles showing theoretical values. Dashed curves are measured results for source impedance $R_s = 100\,\Omega$ with measured $\mathrm{Re}\{Z_{in}\}$ in dotted magenta, measured $\mathrm{Im}\{Z_{in}\}$ in dotted cyan, with $\times$'s showing theoretical values.

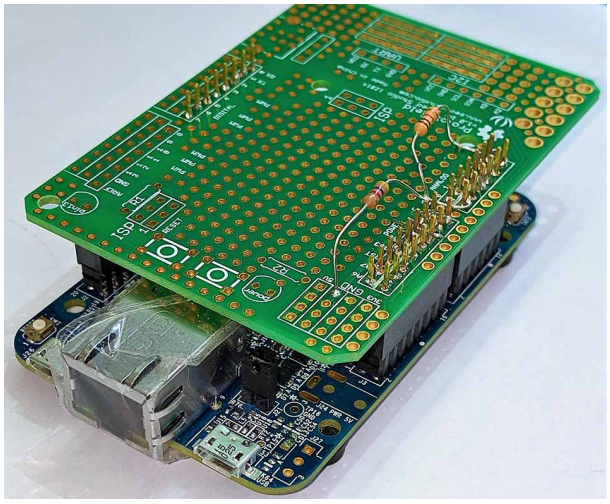

Fig. 7. Prototype using NXP FRDM-K64F microcontroller board on bottom, and with $4700\,\Omega$ R_{adc} and $1000\,\Omega$ R_{io} visible on upper carrier board.

rameter values. In addition, earlier approximations neglecting source impedance, such as given in [4], [9], have previously been experimentally shown to provide good estimates for Z_{in}, and are useful where precise impedances may not be required. The prototype in Fig. 7 seems to operate in such a less-sensitive region. It was constructed using an NXP FRDM-K64F microcontroller board to provide measured results to compare with theory in (4), since this microcontroller has an on-board 16-bit ADC and 12-bit DAC. The prototype was designed for a non-Foster negative capacitance of approximately -8.25 nF in series with 50 ohms, where parameters of Fig. 1 are $R_{adc} = 4700\,\Omega$, $R_{dac} = 1\ \Omega$, $R_{io} = 1000\ \Omega$, and $H(z) = (22z - 19)/(2z + 1)$.

The measured results in Fig. 6 for the prototype suggest that this example may be less sensitive to source resistance variation. The solid curves are measured data for source resistance $R_s = 50\,\Omega$ with measured $\mathrm{Re}\{Z_{in}(s)\}$ in red, measured $\mathrm{Im}\{Z_{in}(s)\}$ in blue, and with circles showing theoretical values. Dotted curves are for source resistance $R_s = 100\ \Omega$ with measured $\mathrm{Re}\{Z_{in}(s)\}$ in dotted magenta, measured $\mathrm{Im}\{Z_{in}\}$ in dotted cyan, and with the $\times$'s showing theoretical values. The source resistance range of R_s from $50\ \Omega$ to $100\ \Omega$ was constrained by instabilities of the prototype outside of this range. At 50 kHz in Fig. 6 changing R_s from $R_s = 50\,\Omega$ to $R_s = 100\,\Omega$, the theoretical digital impedance changed from $Z_{in} = -241 + j424$ to $Z_{in} = -236 + j430$ respectively, and the measured digital impedance changed from $Z_{in} = -282 + j400$ to $Z_{in} = -278 + j404$. The reactance corresponds to the desired $Z = +j386$ for -8.25 nF capacitance, but the large 925 ns latency of this prototype contributed to a large resistive component of Z_{in}. Also, the non-Foster behavior of the negative capacitance is apparent in the negative slope of the reactance between 50 and 100 kHz [8].

The measured data of Fig. 6 is in good agreement with the theory presented, with measured curves close to theoretical expectations, and the measured overall shape of the frequency response in agreement with the theoretical values. The solid red and dotted magenta curves for $\mathrm{Re}\{Z_{in}(s)\}$ in Fig. 6 overlap significantly, in agreement with the overlapping circles and $\times$'s from theory. For $\mathrm{Im}\{Z_{in}(s)\}$, the solid blue curve for $R_s = 50\,\Omega$ is slightly below the dotted cyan curve for $R_s = 100\,\Omega$ in Fig. 6, in agreement with the nearby circles being slightly below the $\times$'s from theory in (4). This change of source resistance only slightly affected the theoretical and measured digital circuit impedance $Z_{in}(s)$, providing an example where $Z_{in}(s)$ may be less sensitive to variations in source impedance than the previous examples. Note that it was not possible to fully measure the upward trend in $\mathrm{Re}\{Z_{in}(s)\}$ at low frequency below 30 kHz due to network analyzer frequency limitations.

V. Summary

Simulation results for two examples, and measured results for a microcontroller prototype of a non-Foster negative capacitance, confirm the theoretical results showing that the input impedance of a digital impedance circuit is dependent on source resistance. The two simulation examples show significant change in digital impedance when source resistance was changed. The measured results illustrate an example where the digital input impedance seems less sensitive to source resistance variation, although only a limited range of source resistance was possible without inducing circuit instability.

Acknowledgment

This material is based upon work supported by the National Science Foundation under Grant No. 1731675.

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