A CMOS Frequency Synthesizer

Final Report

ECGR 6264 Radio Frequency Design

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12/1/2021

YOU MUST COMPLETE ALL OF THE SECTIONS IN THIS TEMPLATE DOCUMENT

The examples below are sparsely filled in for illustration only, and would result in a grade of zero as is. It is not necessary to be verbose, but it is necessary that you provide a complete, but succinct, description in each section.

**Executive summary**

In this project, an integrated circuit Negative Capacitance/Negative Inductance using Negative Impedance Converter is designed. Four separate versions of the design are implemented: cross-coupled amplifier, capacitance to ground, capacitance across drains, and inductance to ground. The design goals in all cases are realize a negative capacitance of -10 pF At 1 GHz.

In the following sections, the design goals are first summarized. Then, schematics of the designs are presented, followed by simulation results. Following this, the layout and pinouts of the design are discussed. Finally, a bibliography is given.

Make sure that your report is sufficiently descriptive and self-contained that anybody could use your report as a manual to test your circuit when it arrives from fabrication.**Design Goals**:

The design goals for the project are to design 4 negative capacitance circuits with:

1. A negative capacitance of -5 pF at 1 GHz using a CMOS negative impedance converter with 2 mA bias and 1 Vpp swing (4 pins, Vdd, + out, -out, bias)
2. A tunable negative capacitance (using a varactor in parallel to the load capacitance) at 1 GHz using a CMOS negative impedance converter with 2 mA bias and 1 Vpp swing (5 pins, Vdd, + out, -out, bias,Vctrl)
3. A negative inductance of -5 nH at 1 GHz using a CMOS negative impedance converter (using one inductor) with 2 mA bias and 1 Vpp swing (4 pins, Vdd, + out, -out, bias)
4. A negative impedance converter with 2 mA bias and 1 Vpp swing (4 pins, Vdd, + out, -out, bias)

Blah, blah, blah…..

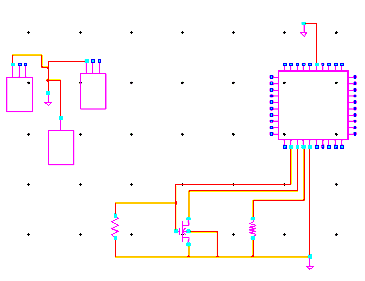
**Cadence Top-Level Circuit Schematics**:

YOU MUST SHOW THE PADFRAME IN THIS SCHEMATIC

The schematic for the top-level of the integrated circuit is given in Fig. x below. Inverter subcircuits X1 and X2 …. connect to the padfreme pins 31 and 32 …The

Blah, blah, blah…..

Fig. x. (a) Schematic of integrated circuit showing padframe and attached subcircuits. Subcircuit X1 is and inverter, Blah, blah…



**ADS Cell Schematics**:

YOU MUST ANNOTATE THE DC SOLUTION

REPEAT THIS SECTION FOR ALL SUBCIRCUITS

The schematic for the inverter is given below. Transistors X1 and X2 implement a current mirror for the differential amplifier comprised of transistors X4 and X5. The

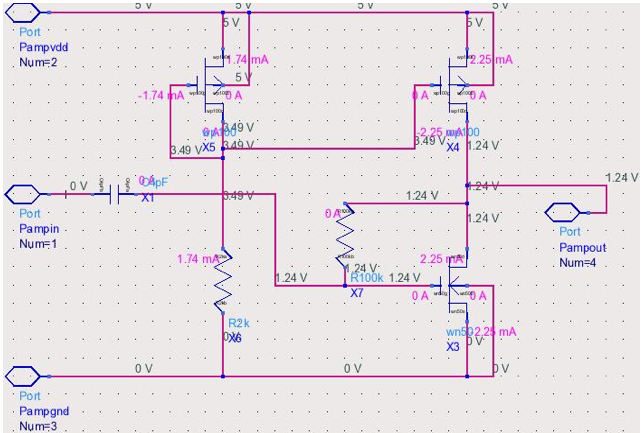
Blah, blah, blah…..

Your paragraphs should describe the function of the devices in the circuit, such as bias circuits, current mirrors, amplifiers, active loads, feedback, etc.

Do not forget to describe the function and purpose of each port, such as… port vin is the amplifier input port, etc….

**Cadence Cell Schematics**:

Fig. x. Schematic of inverter subcircuit. Transistors X1 and X2 comprise the current source for differential amplifier transistors X3 and X4. Blah, blah…



YOU MUST ANNOTATE THE DC SOLUTION

REPEAT THIS SECTION FOR ALL SUBCIRCUITS

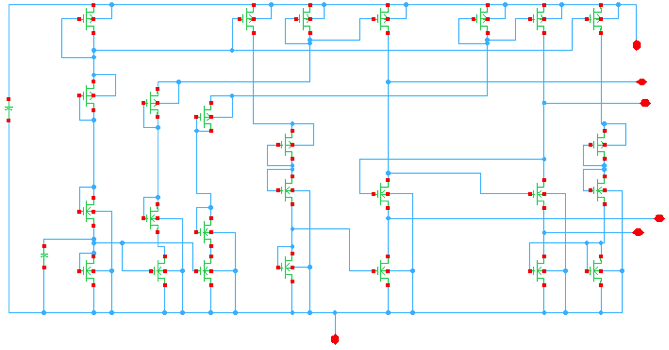
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**ADS Test Circuit Schematics**:

YOU MUST ANNOTATE DC SOLUTION!!

REPEAT THIS PAGE FOR AS MANY MEASUREMENTS SETUPS AS NEEDED TO VALIDATE YOUR PARTICULAR PROJECT

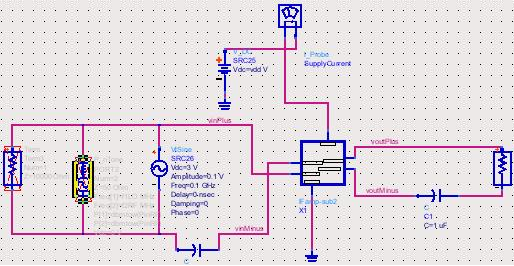
The schematic for the OIP3 test circuit is given in Fig. x below. A two-tone source at 100 and 101 MHz is applied to the input, and Harmonic Balance analysis is performed.. The

Blah, blah, blah…..

Your paragraphs should describe the function of the devices connected to your circuit, terminations, power supplies, signal sources, feedback, etc.

**ADS Simulation Results**:

Fig. x. Schematic of OIP3 test circuit. A two-tone input at 100 MHz and 101 MHz ia applied at the input. Fundamental and third-order distortion are measured at the output. Blah, blah…



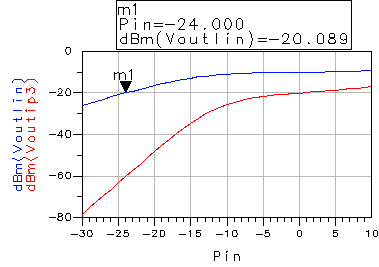
REPEAT THIS PAGE FOR AS MANY MEASUREMENTS AS NEEDED TO VALIDATE YOUR PARTICULAR PROJECT

The third order intercept data in Fig. x below shows the nonlinearity of the negative capacitance at 101 MHz.

Blah, blah, blah…..

Your paragraphs should describe the results and compare them to the design goals, such as “the resulting OIP3 from the simulation below is +14 dBm, and is 1 dB above the design goal of +13 dBm…”

Fig. x. Simulation results showing third order intercept at 100 MHz from harmonic balance analysis.



**Cadence Test Circuit Schematics**:

YOU MUST ANNOTATE DC SOLUTION!!

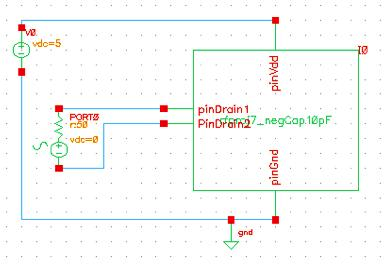
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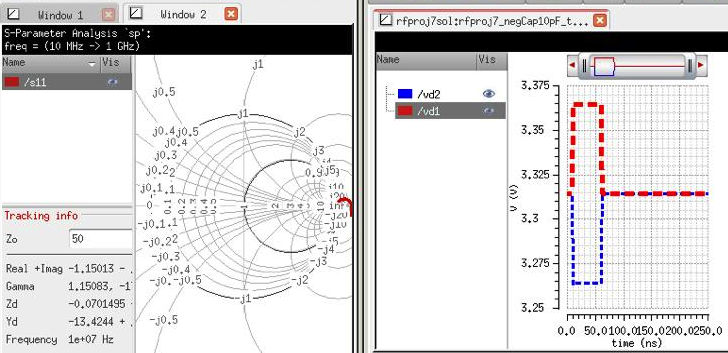
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Fig. x. Simulation results showing third order intercept at 100 MHz from harmonic balance analysis.



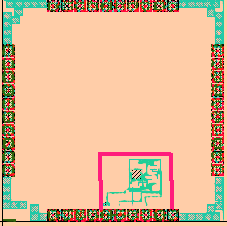
**Cadence Layout**:

Fig. x below shows the layout of the integrated circuit. The lower right portion is the …..

Blah, blah, blah…..

Your paragraphs should describe the location of the major subcircuits in the layout below.

Fig. x. Final integrated circuit layout. Inverting amplifier is in red box shown at lower right of the integrated circuit layout.



**Pinout**:

The table below shows pinout assignment for the integrated circuit.

Blah, blah, blah…..

The table below should list all pins used in your design, and provide sufficiently descriptive descriptions of each pin. This information will be needed to test your circuit when it arrives after fabrication.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin | Description | In/out | Dc input bias | DC out  expected |
| 21 |  |  |  |  |
| 22 |  |  |  |  |
| 23 |  |  |  |  |
| 24 |  |  |  |  |
| 25 |  |  |  |  |
| 26 |  |  |  |  |
| 27 | Not used |  |  |  |
| 28 | Vdd for the inverting amplifier (+5 volts DC) | in | 5 V, 11 mA |  |
| 29 | Amplifier input for third inverter subcircuit | in | 1.5 V |  |
| 30 | Gnd ; Substrate ground pin | in | 0 |  |
| 31 | Inductor output of negative inductance circuit | in | 0 |  |
| 32 | Not used |  |  |  |
| 33 | Amplifier output | out |  | 2.2 V |
| 34 |  |  |  |  |
| 35 |  |  |  |  |
| 36 |  |  |  |  |
| 37 |  |  |  |  |
| 38 |  |  |  |  |
| 39 |  |  |  |  |
| 40 |  |  |  |  |

**Bibliography**:

1. R. Brennan, T. Viswanathan, and J. Hanson, “The cmos negative impedance converter,” Solid-State Circuits, IEEE Journal of, vol. 23, no. 5, pp. 1272–1275, Oct. 1988. <http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5957>
2. Reja, M.M.; Moez, K.; Filanovsky, I.; “A wide frequency range CMOS active inductor for UWB bandpass filters,” . 52nd IEEE International Midwest Symposium on Circuits and Systems, 2009. <http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5235983>
3. Negative Impedance Circuit and Its Application to Inductorless Resonant Oscillators, <http://cad.yonsei.ac.kr/conference/international/IC_45.pdf>
4. Guang Fei Zhang, C.S.Ripoll,J.L.Gautier, M.L.Villegas, “Broadband Lossless Monolithic Microwave Floating Active Inductor,” IEEE International Symposium on [Circuits and Systems, 1993., ISCAS '93, 1993](http://ieeexplore.ieee.org/xpl/mostRecentIssue.jsp?punumber=1067) . <http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=393919>