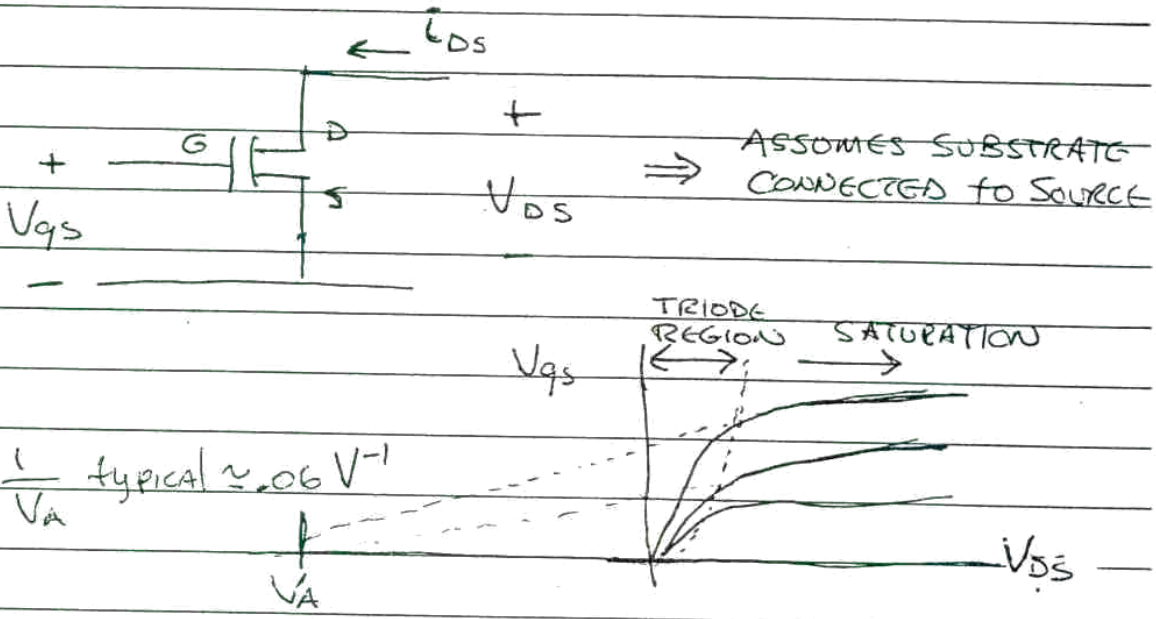
CMOS
REVIEW

CHECK TEXTBOOK TO CORRECT
ANY ERRORS.

TWEEDON

Review Notes I

N-channel Enhancement Mode MOSFET



$\lambda = \frac{1}{V_A}$ typical $\simeq .06\ V^{-1}$

In Saturation Region $V_{DS} \geq V_{gs} - V_T$

$$i_{DS} = \frac{W}{L}\frac{k_p}{2}\left(V_{gs} - V_T\right)^2\left(1 + \lambda V_{DS}\right)$$

W, L = gate width & length, V_T = Threshold Voltage $\simeq .8V$

$k_p = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}} \simeq \frac{4\mu_n \varepsilon_0}{t_{ox}}$ = Process Transconductance

C_{ox} = capacitance/unit area, μ_n = Electron mobility

t_{ox} = oxide thickness, typical $k_p \simeq 20\mu A/V^2$

Output Resistance $= \frac{1}{d i_D / d v_{gs}} \simeq \frac{1}{\lambda i_{DS}} = R_{DS}$

Note: $\frac{k_p}{2}$ = MOSIS K' in process data

(λ = channel length modulation param.)

IN TRIODE REGION. $V_{DS} < V_{GS} - V_T$

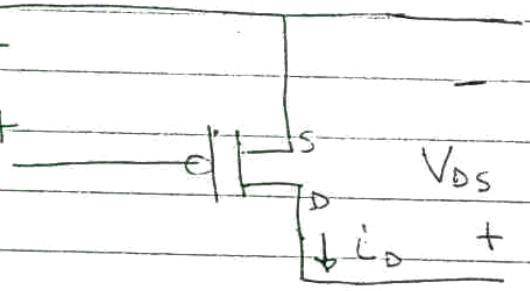
$$i_{DS} = k_p \frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$$

here DRAIN-SOURCE BEHAVES LIKE A VOLTAGE VARIABLE RESISTOR where

$$R_{DS} = \frac{1}{k_p \frac{W}{L}(V_{GS} - V_T)}$$

SIMILARLY

ENHANCEMENT MODE PFET



BOOK USES DIFFERENT CONVENTION!

Note: Different direction, i_D "OUT" of DRAIN

Also V_T AND V_{GS} ARE TYPICALLY NEGATIVE

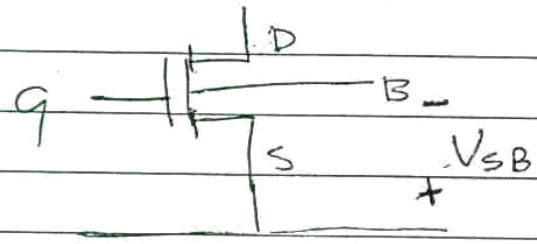
$$i_D = \frac{W}{L}\frac{k_p}{2}(V_{GS} - V_T)^2(1 + |\lambda V_{DS}|)$$

Body Effect

IF SOURCE IS NOT CONNECTED TO BULK

$$V_T = V_{TO} + \gamma\left(\sqrt{|2\phi_s| + V_{SB}} - \sqrt{|2\phi_f|}\right)$$

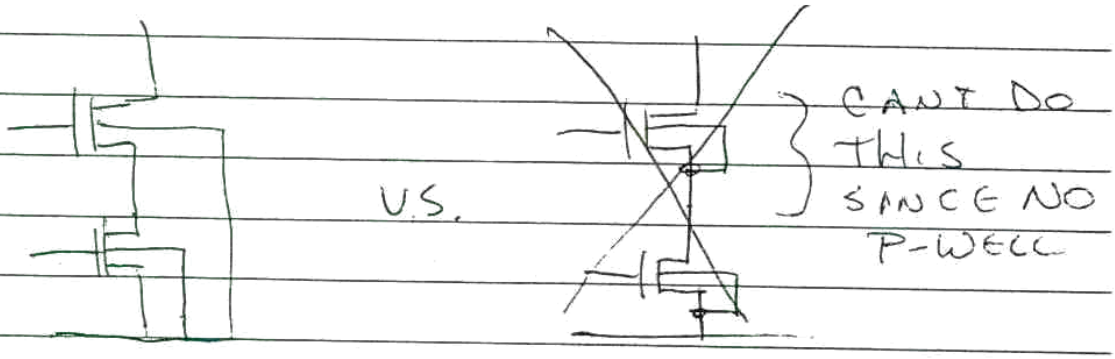
↑ NORMALLY POSITIVE FOR N-CHANNEL



$\phi_f \approx -.3V$

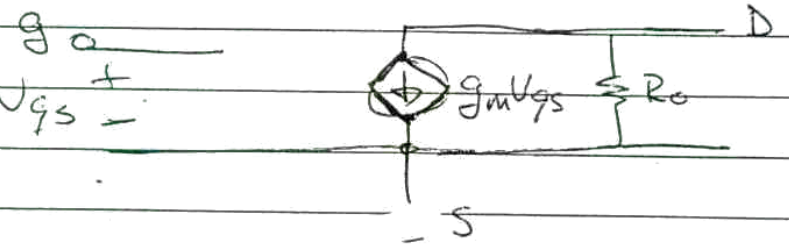
So V_T INCREASES AS V_{SB} INCREASES.

CONSIDER



IN OUR PROCESS ALL NFETS BULK IS GROUNDED SO! LEFT CASE HOLDS!

Small Signal Models



In Saturation

$$g_m = \frac{d i_D}{\partial V_{gs}} = \frac{W}{L} k_p (V_{gs} - V_T)(1 + \lambda V_{DS})$$

$$\approx \frac{W}{L} k_p (V_{gs} - V_T)$$

$$= \sqrt{2 \frac{W}{L} k_p i_D}$$

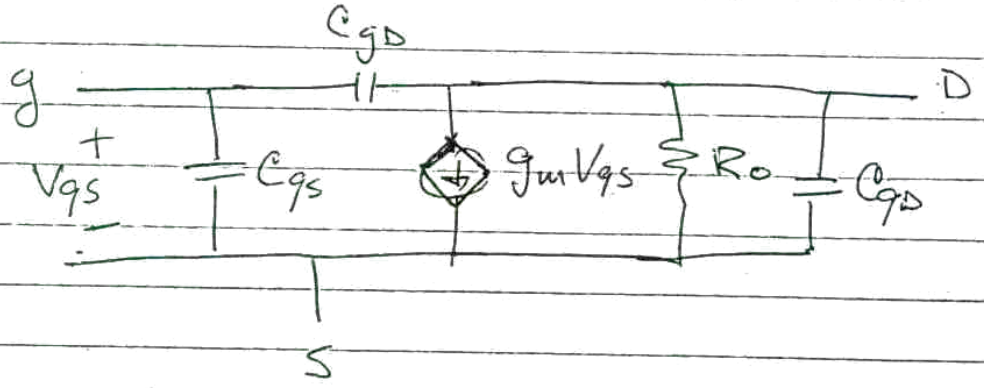
And

$$R_o = \frac{1}{\lambda I_{DS}}$$ as before.

Another useful form, where $i_D \approx \frac{W}{L} \frac{k_p}{2} (V_{gs} - V_T)^2$

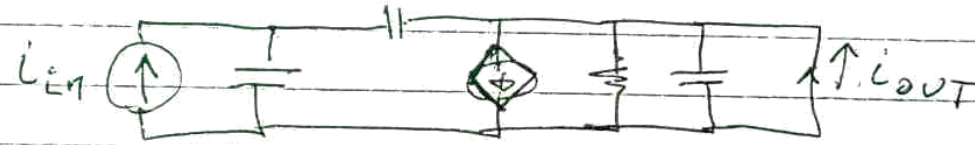
$$g_m \approx \frac{W}{L} k_p (V_{gs} - V_T) = \frac{2 i_D}{V_{gs} - V_T}$$

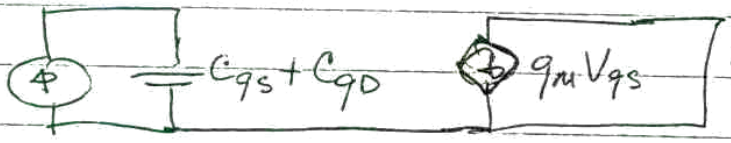
Adding Capacitances



Consider

① Current Source in ② short circuit out





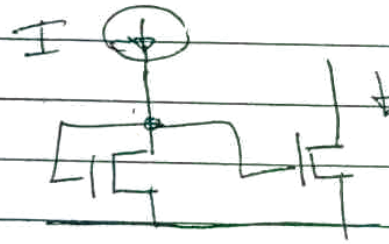
$$\frac{i_{OUT}}{i_{IN}} = \frac{g_m V_{gs}}{i_{IN}} = \frac{g_m \overbrace{\frac{i_{IN}}{j\omega(C_{gs}+C_{gD})}}}{i_{IN}} = \frac{g_m}{\omega(C_{gs}+C_{gD})}$$

Unity Gain Frequency Figure of Merit

$$f_T = \frac{\omega_T}{2\pi} = \frac{g_m}{2\pi(C_{gs}+C_{gD})}$$

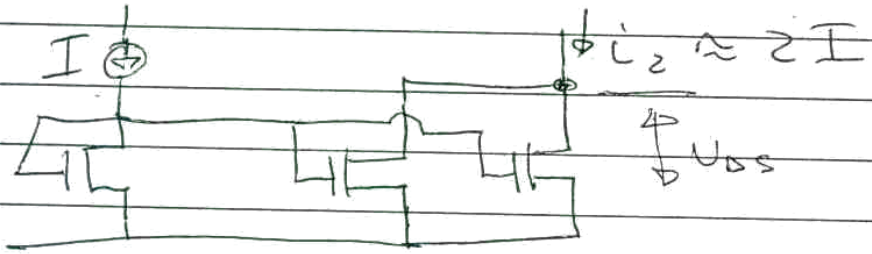
CMOS Circuits

Current Mirror



if $\frac{W}{L}$ SAME FOR BOTH DEVICES

(ACTUALLY $i_2 = \frac{k_p}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS})$



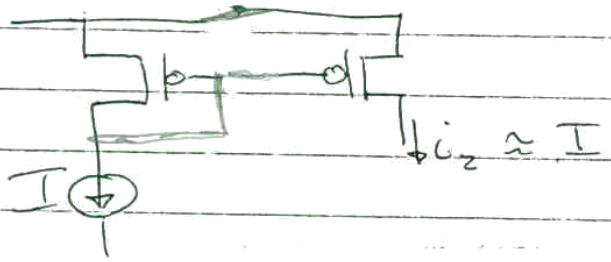
IN ABOVE, "MINIMUM VOLTAGE" OF USEFUL RANGE IS WHEN OUTPUT FET IS IN SATURATION, i.e.

KEEP $V_{DS} \geq V_{GS} - V_T$ AT output

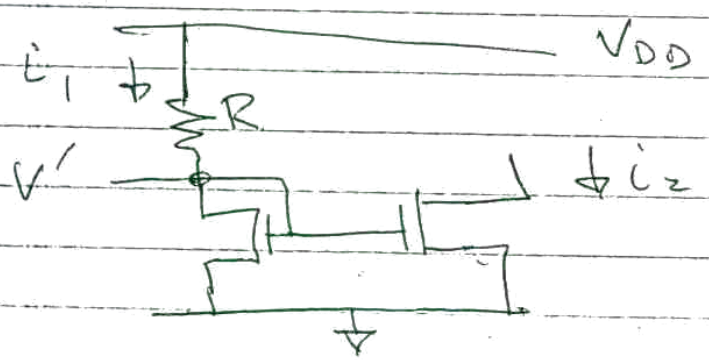
IN FIRST CASE ABOVE, note

$$R_o \simeq \frac{1}{\lambda i_2}$$

OTHER CURRENT SOURCES!



EXAMPLE SIMPLIFIED ANALYSIS

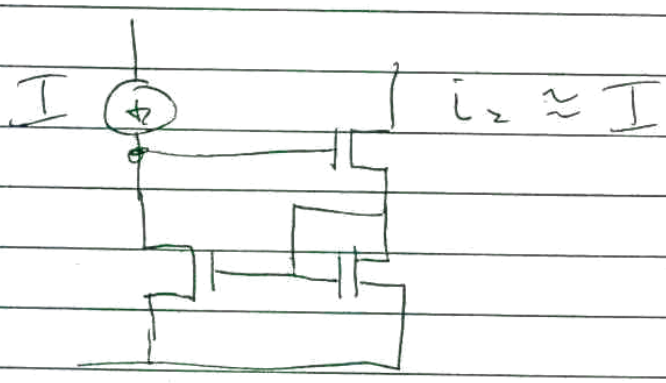


if R is VERY LARGE, $V' \simeq V_T$

So $i_1 \simeq \frac{V_{DD} - V_T}{R} \simeq i_2$

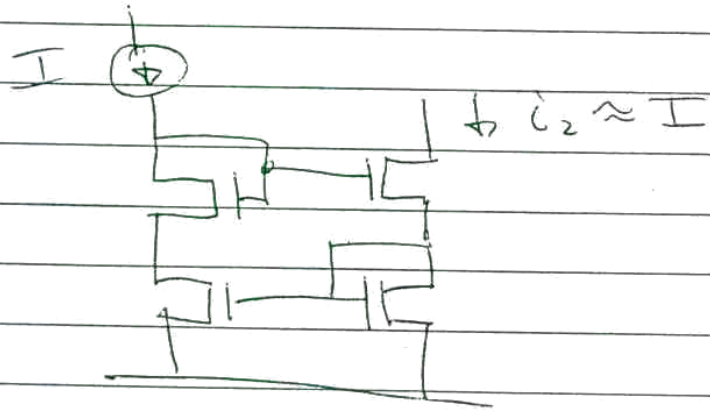
Higher output impedance source

(Wilson Current Mirror)



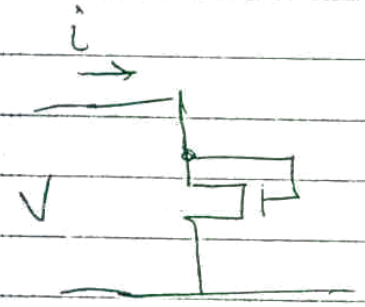
Disadvantage: output voltage must be higher to bias 2 devices in output.

Even Better (Modified Wilson)



Note

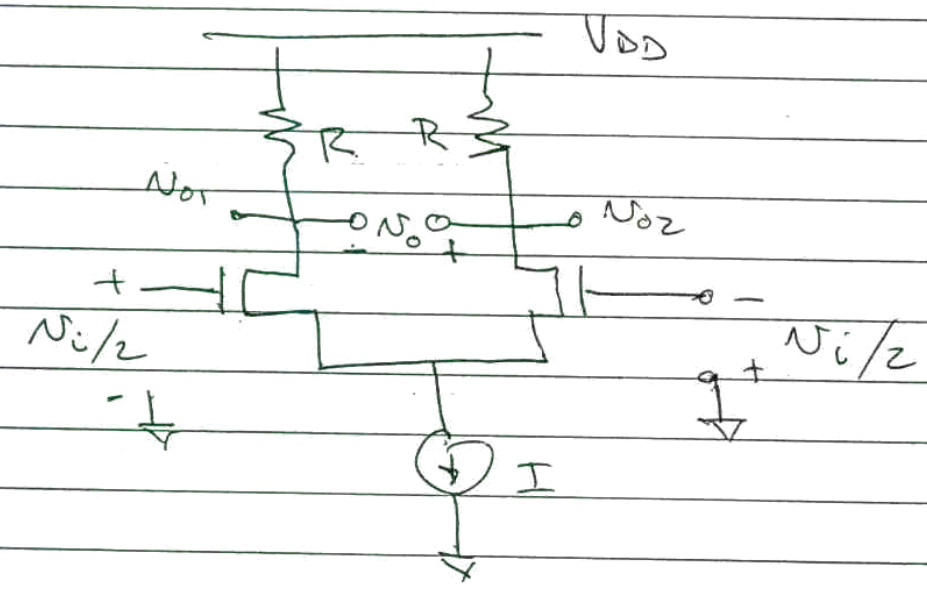
"Diode Connected" FET



Above V_T; $V > V_T$
FET is "ON" ($i > 0$)

Below V_T; $V < V_T$
FET is "OFF" ($i = 0$)

Differential Amplifier



$v_{o1} = -g_m(R \| r_o)\frac{v_i}{2}$ $\quad r_o$ = FET OUTPUT RESISTANCE

$v_{o2} = -g_m(R \| r_o)\left(\frac{-v_i}{2}\right)$ $\quad = \frac{1}{\lambda i_D} = \frac{2}{\lambda I}$

$v_o = v_{o2} - v_{o1} = g_m(R \| r_o)\, v_i$

DIFFER. GAIN $= \frac{v_o}{v_i} = g_m(R \| r_o)$

Recall $g_m \approx \frac{W}{L} k_p (v_{GS} - V_T) = \sqrt{2\frac{W}{L} k_p i_D}$

$= \frac{2 i_D}{v_{GS} - V_T}$

So

DIFF GAIN $\approx \sqrt{\frac{W}{L} I k_p}\,(R \| r_o) = \underline{\frac{I\,(R \| r_o)}{v_{GS} - V_T}}$

Since $r_o \approx \frac{2}{\lambda I}$

$$\text{Diff Gain} = \frac{N_o}{N_i} = \frac{I(R \| r_o)}{V_{gs} - V_T} = \frac{I\left(R \| \frac{2}{\lambda I}\right)}{V_{gs} - V_T}$$

Max Gain is $R \to \infty$, $R \| \frac{2}{\lambda I} \Rightarrow \frac{2}{\lambda I}$

$$\text{Max Gain} = \frac{2}{\lambda (V_{gs} - V_T)}$$

Similarly

$$\text{Diff Gain} = \sqrt{\frac{W}{L} k_p I}\,(R \| r_o) = \sqrt{\frac{W}{L} k_p I}\left(R \| \frac{2}{\lambda I}\right)$$

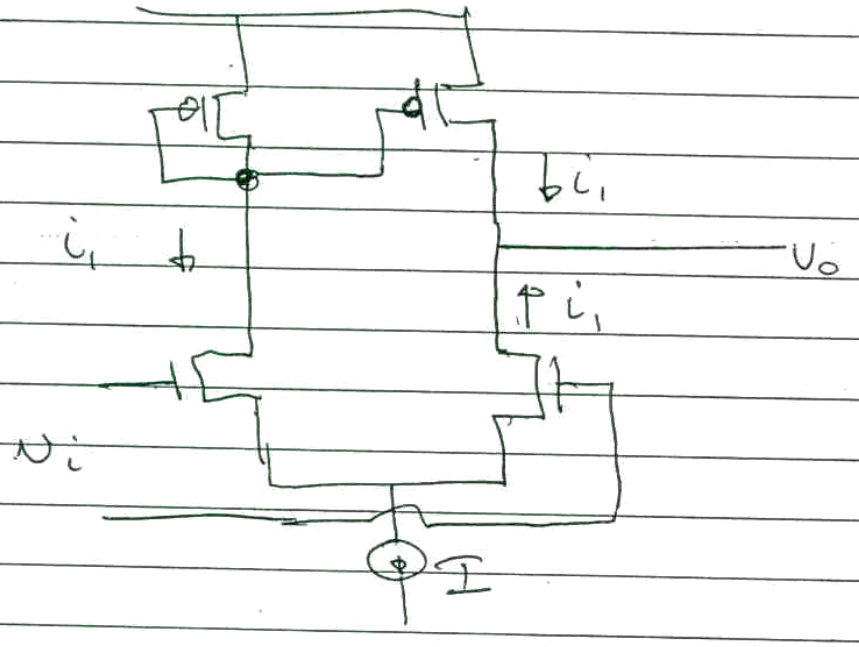
$$\text{Max Gain} \approx \sqrt{\frac{W}{L} k_p I}\left(\frac{2}{\lambda I}\right)$$

$$= \sqrt{4 \frac{W}{L} k_p \left(\frac{1}{I}\right)\left(\frac{1}{\lambda^2}\right)}$$

So Higher Gain's

- Increase W/L
- Reduce I

Active Load



Current mirror drives i_1 down on right top so get 2x current.

However, get $\frac{1}{2}$ voltage since output here isn't differential (it is single-ended)

So these two effects cancel

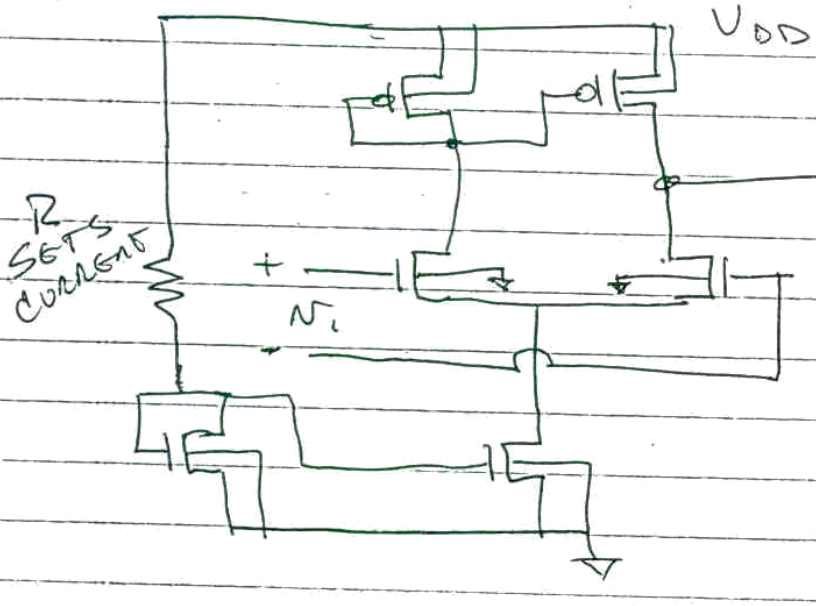
Finally $R = r_o$ since it is replaced by the upper FET

$$\text{So} \Rightarrow \text{Gain} = \frac{V_o}{V_i} = g_m(r_o \| r_o) = g_m \frac{r_o}{2}$$

$$= \frac{1}{\lambda(V_{gs} - V_T)} = \frac{1}{\lambda I}\sqrt{\frac{W}{L} k_p I}$$

$$= \sqrt{\frac{W}{L} k_p \left(\frac{1}{\lambda^2 I}\right)}$$

Implementation

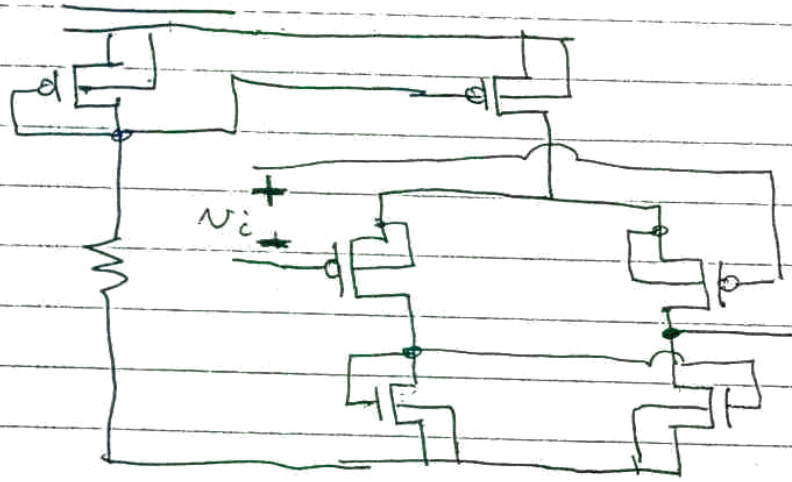


⟸ NFETS MUST HAVE BULK GROUNDED IN OUR PROCESS

SO

BULK EFFECT ON V_T

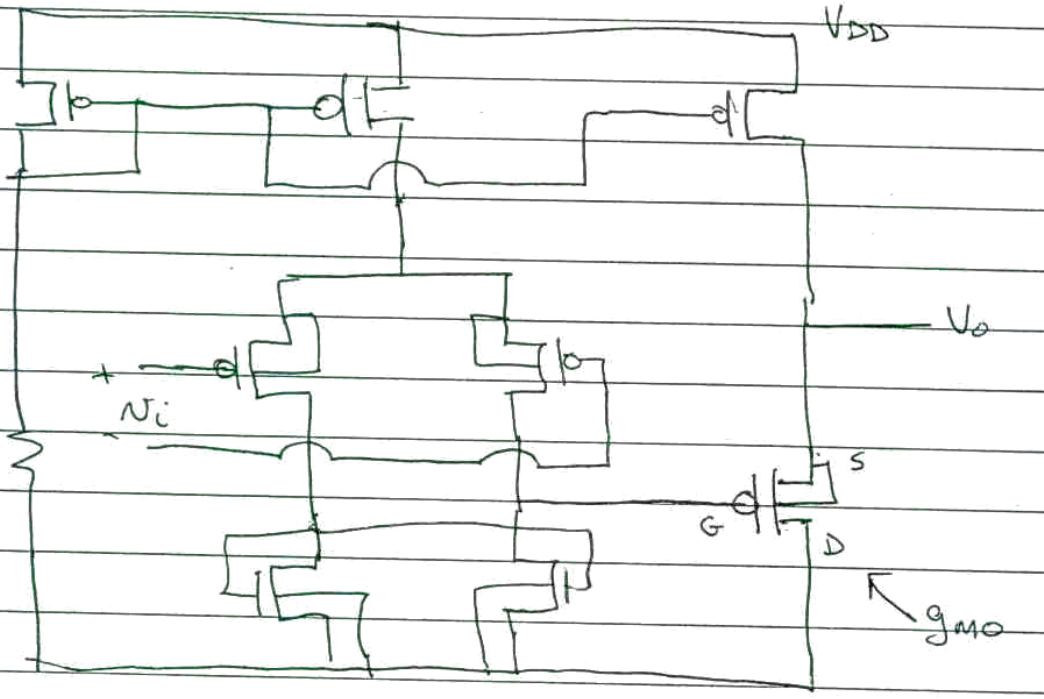
BETTER



ALL DEVICES BULK CONNECTED TO SOURCE.

Finally

ADD SOURCE FOLLOWER W/ACTIVE LOAD



SOURCE FOLLOWER

GAIN $\simeq 1$

$R_{OUT} \simeq \frac{1}{g_{mo}}$

$\Rightarrow$ LOWER OUTPUT IMPEDANCE

$\Rightarrow$ LARGER BANDWIDTH.

(DRIVING CAPACITANCE.)

Simple Bias Scheme

BIAS

Amplifier