PROJECT ON MIXED SIGNAL VLSI

Submitted by

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TOPIC: A GILBERT CELL MIXER IN CMOS AND BJT TECHNOLOGY

A Gilbert Cell Mixer in CMOS and BJT technology

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Abstract – This paper describes a doubly balanced Gilbert Cell mixer designed in BJT and CMOS technology to operate within 0 to 5 V. A 100 mv input signal was applied at both RF and LO port at different frequencies and their simulation curves were studied for a multiplier. The design done in BJT was taped out for fabrication and the chip on its return from foundry, was tested for its results. A comparison of theoretical and experimental results obtained after fabrication of the Four-Quadrant Gilbert cell mixer in 2-micron process is made. For CMOS process, Gilbert cell mixer was designed till the layout and was ready for handoff to the foundry. The chip was not fabricated in CMOS technology, but the output results were studied and compared in both BJT and CMOS technology.

1. Introduction

The Gilbert Cell Mixer is very useful building blocks in transceiver design. The design of mixers forces many compromises between conversion gain, local oscillator (LO) power, linearity, noise figure, port-to-port isolation, voltage supply and current consumption [1]. Bipolar variable – transconductance multiplier based on Gilbert Cell have been successfully used for many years [2]. Unfortunately, it is not possible to realize a CMOS multiplier simply by substituting the BJT's in a bipolar multiplier with CMOS transistors as is often done in developing the CMOS functional equivalent of established bipolar circuits. This is due to the fact that the output current of the CMOS source-coupled differential pair depends nonlinearly on the bias current Iss and input signal [2]. Consequently, the linear input range of the corresponding CMOS four quadrant Gilbert cell multiplier is narrow and difficult to compensate.

The most fundamental choice is FET mixer design is whether to use active or a passive mixer. Active FET mixers achieve conversion gain and require lower LO power than their passive counterparts [1]. Passive FET mixers (operating FET's in the linear region) are a well known mixing technique; they typically demonstrate conversion loss and excellent intermodulation performance at the expense of LO power [1].

A reduced LO drive is a significant advantage in low-voltage / low-power IC design because large LO drives are difficult to generate in a low-voltage environment and results in an increase in power dissipation [1]. This also dictates increased LO-RF/LO-IF isolation in order to maintain the same rejection as would be obtained with a lower LO drive. The primary advantage of a passive mixer is increased in dynamic range at the expense of LO drive.

Doubly balanced mixers have inherent port-to-port isolation making the doubly balanced structure ideal for integrated circuit design [3]. The doubly balanced bipolar

Gilbert cell mixer is favored in integrated circuit applications [4]. A typical Gilbert cell mixer has a stack of three transistors and load resistors between the voltage rails. As the voltage supply is reduced, it is important to maintain dynamic range for transceiver performance. This paper investigates the low voltage performance of a CMOS and BJT Gilbert mixer to demonstrate CMOS as a potential RF technology.

An active doubly balanced mixer with cascoded N-channel and P- channel devices in a Gilbert topology [5] takes the advantage of excellent current reuse. However, the use of P-channel device in the RF stage limits the frequency of operation. A doubly balanced Gilbert cell mixer design for a zero IF receiver [6] uses P-channel current sources for the IF load. P-channel current sources are unsuitable in a traditional –heterodyne architecture with a high intermediate frequency, because the poor transconductance (gm) of P-channel devices results in physically large P-channel devices. These devices have large shunt capacitance that attenuate high IF signals. Active mixers with resistive loads enable a high IF frequency for down-conversion [7] and make excellent up-converters.

II. Circuit Description and Operation

A doubly balance BJT and CMOS mixer was designed based on a Gilbert cell topology [3] as shown in Fig 1. (a) – BJT version and Fig 1. (b) – CMOS version [1]. The RF and LO ports were biased internally employing the diode connected transistors. Resistors of 1 KΩ and 100 Ω were employed for biasing the BJT version of Gilbert cell mixer whereas the CMOS version was biased using active loads. The current consumption of the mixer was controlled by current mirrors that regulated current to the Gilbert cell mixer and to an output buffer.

Fig1. (a) Shows Gilbert cell mixer in BJT technology employing passive components like resistors, diode connected transistors for biasing, and emitter coupled differential pair and four cross-coupled devices. The transistors Q5 and Q6 form emitter coupled differential pair. Operation of differential amplifier is best understood by dividing the RF signal into its common mode and differential mode components. The RF signal enters one side of the pair while the opposite side is AC grounded through a capacitor. From symmetry, the common mode component has no first order effect on the output voltage. The differential mode component shifts the current between the two branches, and for the small signal acts as a standard common emitter amplifier. The transistors Q1, Q2, Q3 and Q4 are four cross-coupled devices with LO input provided to the base of Q4 employing coupling capacitor Cc. The collector of transistor Q1 and Q3 are connected together because the currents in their respective collector are in same phase. Same is the case for transistors Q2 and Q4. A LO signal is used to switch the conduction path between the outer and inner transistors of the cross-coupled quad, creating the mixing action.

The coupling capacitor is used externally to avoid the RF/LO input from propagating to the other end. It also provides the necessary isolation between ports. The bases of transistors Q2 and Q3 are AC grounded to serve the purpose of single ended LO input. The combination of these devices with the emitter coupled differential pair

completes the basic Gilbert cell. Transistor Q7 is used as an emitter follower, which is used to reduce loading effects at the output port. The IF output is taken at the emitter of transistor Q7 using a coupling capacitor. Constant current is provided to the Gilbert cell mixer by employing current mirror rail.
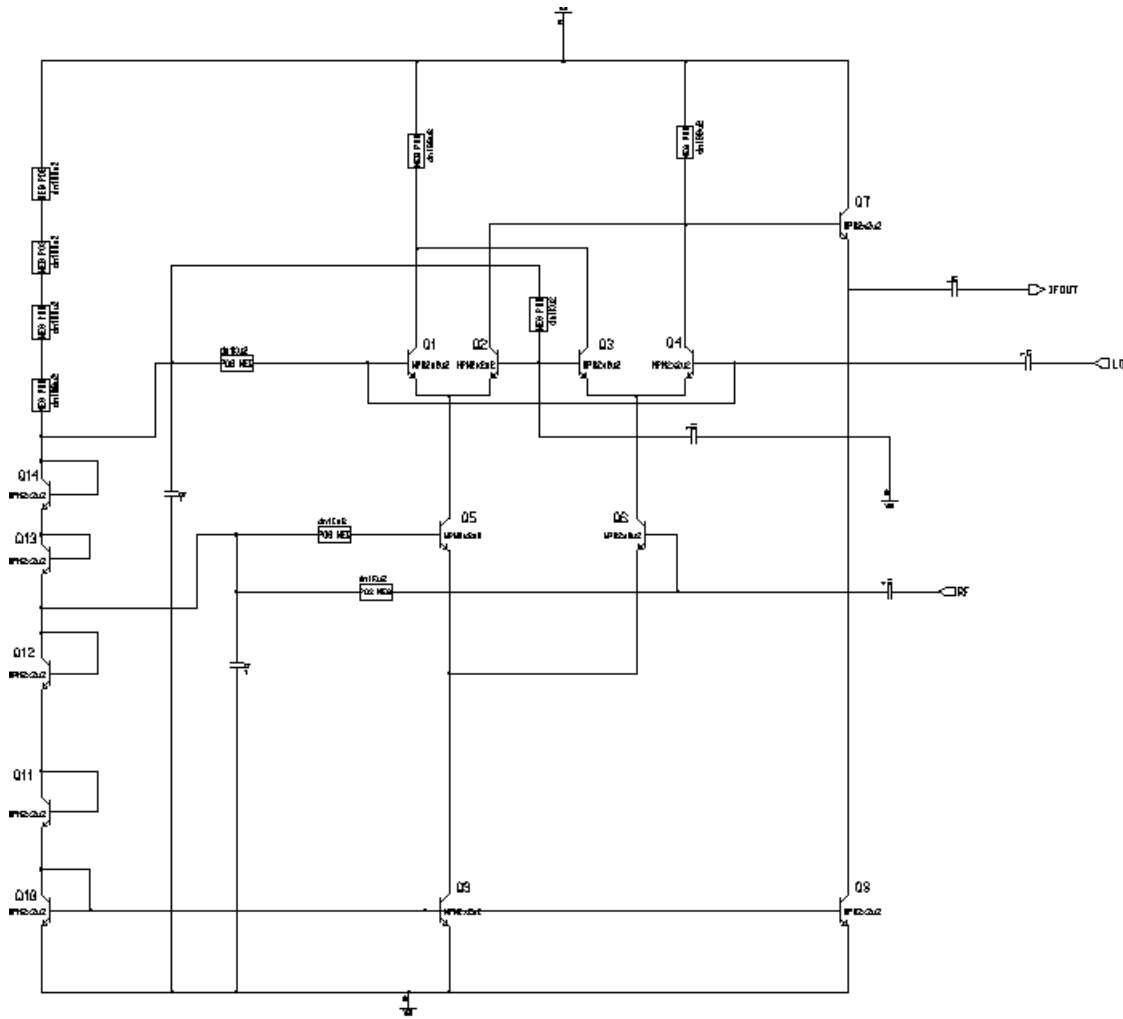
Fig 1. (e)

GILBERT FOUR QUADRANT MULTIPLIER USING BJT's - SCHEMATIC

Transistors Q8, Q9 and Q10 form the current mirror. To ensure the proper working of the circuit transistors Q8, Q9 and Q10 should always operate in active region. For the device conduction, active Gilbert cell mixer requires a DC power supply. DC bias is applied in the form of Vdd of 5V. Enough voltage must be applied to cause the transistors in the Gilbert cell to conduct; otherwise the desired switching action will not occur.

Transistors Q11, Q12, Q13 and Q14 are diode connected transistors (base connected to the collector to provide a drop of 0.7 V across the device) connected to Vdd

of 5 V supply voltage via the 400 Ω resistors. This provides fixed biasing internally for the four-cross devices and the emitter coupled differential pair. Since changes in bias effect linearity, such changes alter the levels of harmonic and spurious signals produced by the Gilbert cell. Biasing changes also effect the frequency range over which the mixer operates. To avoid the changes in biasing we have used fixed biasing. It also ensures that the transistors employed for current mirror rail are operating in active region. To avoid the mismatches at any port, the RF/LO ports are well terminated and both the inputs are single ended.

Since the chip was fabricated in BJT technology, the collector current equations for the cross-coupled devices are as below:

$$I_{c1} = \frac{I_{c5}}{1 + e^{(\frac{-V_{LO}}{V_T})}} \qquad\qquad 1$$

$$I_{c3} = \frac{I_{c6}}{1 + e^{(\frac{-V_{LO}}{V_T})}} \qquad\qquad 2$$

$$I_{c2} = \frac{I_{c5}}{1 + e^{(\frac{V_{LO}}{V_T})}} \qquad\qquad 3$$

$$I_{c4} = \frac{I_{c6}}{1 + e^{(\frac{V_{LO}}{V_T})}} \qquad\qquad 4$$

The collector current for the emitter coupled differential pair is given below:

$$I_{c5} = \frac{I_{EE}}{1 + e^{(\frac{-V_{RF}}{V_T})}} \qquad\qquad 5$$

$$I_{c6} = \frac{I_{EE}}{1 + e^{(\frac{V_{RF}}{V_T})}} \qquad\qquad 6$$

The output current is as below:

$$\Delta I = (I_{c1} + I_{c3}) - (I_{c2} + I_{c4}) = I_{EE}\left[\tanh\left(\frac{V_{LO}}{2V_T}\right)\right]\left[\tanh\left(\frac{V_{RF}}{2V_T}\right)\right] \qquad\qquad 7$$

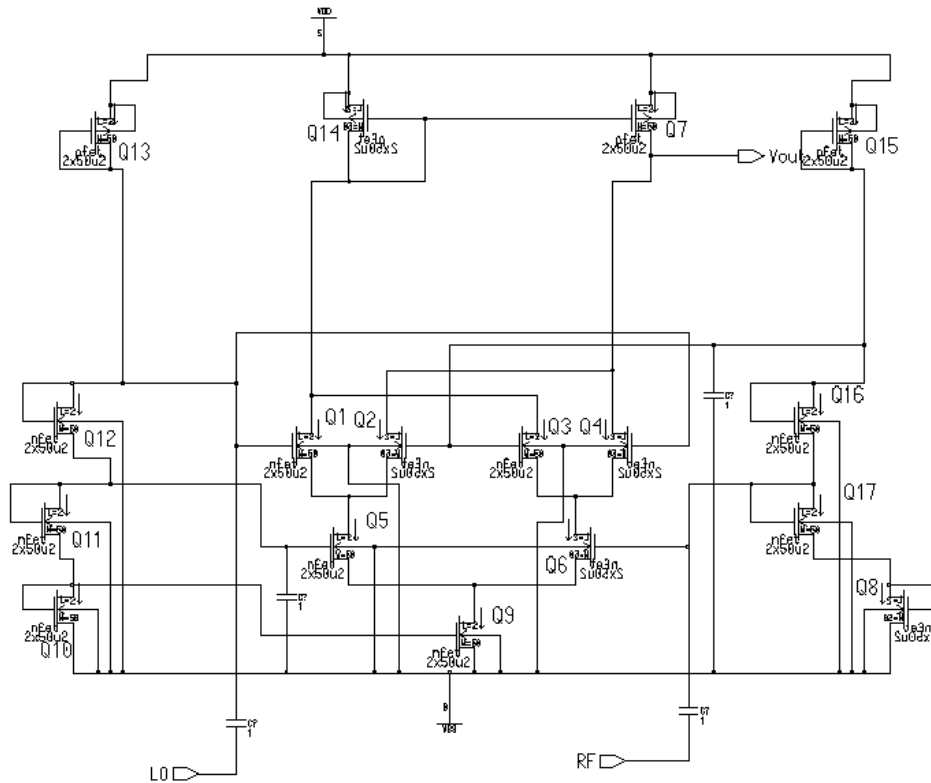$$\Delta I \approx \frac{I_{EE}}{4V_T{}^2} V_{LO} V_{RF}$$

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Fig 1.(b)

GILBERT FOUR QUADRANT MULTIPLIER USING CMOS - SCHEMATIC

Fig1. (b) Describes Gilbert cell mixer in CMOS technology using P-channel devices as current source and N-channel devices as current mirror, active load, differential amplifier and four cross-coupled devices. The N-channel devices Q5 and Q6 form source coupled differential pair. The RF input is single ended which is applied to the gate of device Q6 with the other end AC grounded through the capacitor. The Fets Q1, Q2, Q3 and Q4 are four cross-coupled N-channel devices with LO input injected in a single ended fashion to the gate of device Q1 employing coupling capacitor Cc. The coupling capacitors are used externally to avoid the RF/LO input from propagating to the other end. It also provides the necessary isolation between ports. Here the gates of devices Q1 and Q4 are connected to the LO port and the gates of devices Q2 and Q3 are AC grounded. The combination of these devices with the source coupled differential pair completes the basic Gilbert cell.

The N-channel devices namely Q8, Q9 and Q10 provide the necessary current for the working of the Gilbert cell. The current rail also provides necessary current for the Gilbert cell to operate in saturation region and to switch on and off. The fixed biasing is provided internally by the active P-channel and N-channel devices. The Fets Q11, Q12, Q16 and Q17 are N-channel active load and Fets Q13 and Q15 are P-channel active load. The active devices along with the current rail help the Gilbert cell to operate in saturation region. The RF/LO inputs to the N-channel devices were single ended and capacitors of 1 farad was used externally to avoid input from propagating to the other end. The IF output is taken at the drain of device Q7 in a single ended fashion.

The length and width of all the Fets are of 2 microns and 50 microns.

III. Simulations

The RF input (+/- 100 mv) and the LO input (+/- 100 mv) are injected in single ended fashion to the Gilbert cell with the opposite side AC grounded through the external capacitors. The four-quadrant multiplier is used to multiple the RF signal at LO rates. The positive LO voltages causes the outer devices Q1 and Q4 to be ON while the negative LO voltages causes the inner devices Q2 and Q3 to be ON. The operation of transistors Q8, Q9 and Q10 in active region ensures the proper switching of currents from outer devices, Q1 and Q4 (while LO is positive) to inner devices, Q2 and Q3 (while LO is negative).
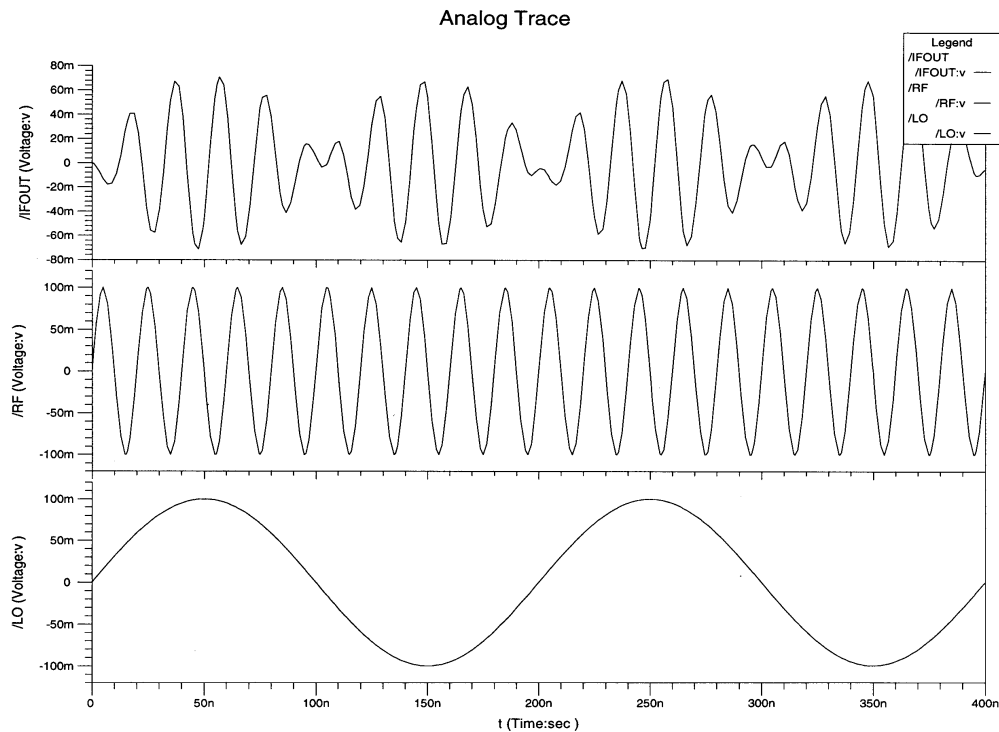

Fig 2. (a)
Simulation Curve for BJT

The simulation curves can be best understood by considering the input and output simulations curves for Analog and digital LO. The input at the RF port was injected at different frequencies starting from 10 MHz upto 500 MHz. Likewise, the input at the LO port was injected at different frequencies starting from 10 MHz to 500 MHz. Fig 2. (a) Shows the simulations curve for BJT technology. A 100mv RF input signal at 100 MHz is applied at the RF port and 100 mv LO signal at 10 MHz is applied at the LO port. The IF output curve shows that the mixer is a downconverter i.e. the (IF) frequency is lower than the input (RF) signal.

The Fig 2. (b) Shows the simulation curve for CMOS technology. A100 mv RF/LO input at 100 MHz and 10 MHz is applied at the RF/LO port. The output curve shows that the active Gilbert cell mixer is a downconverter.
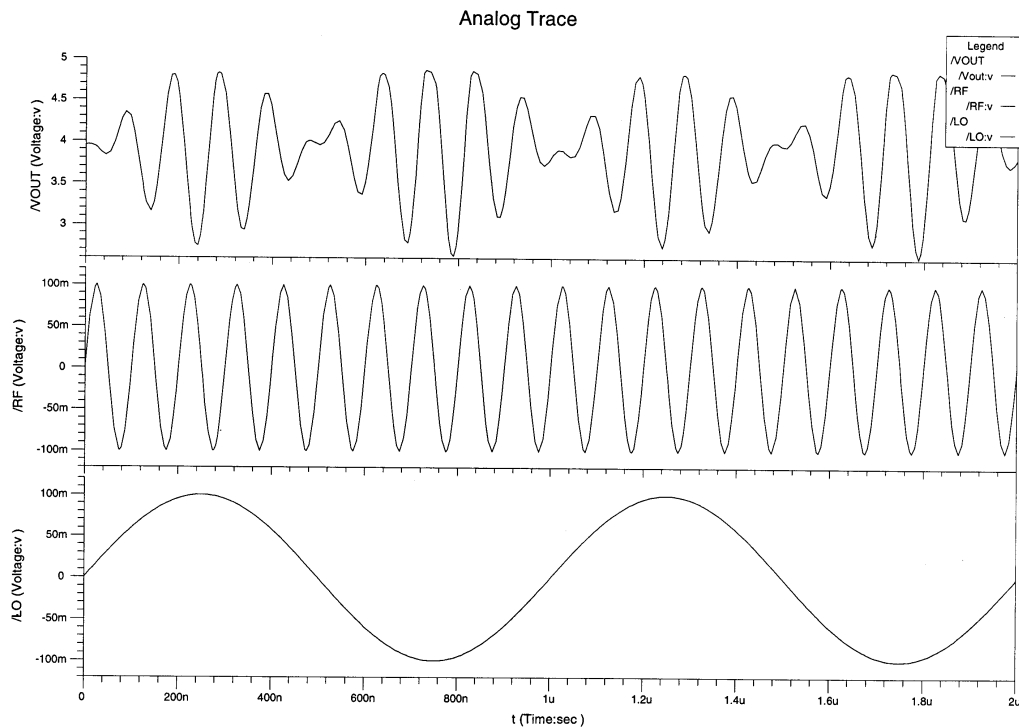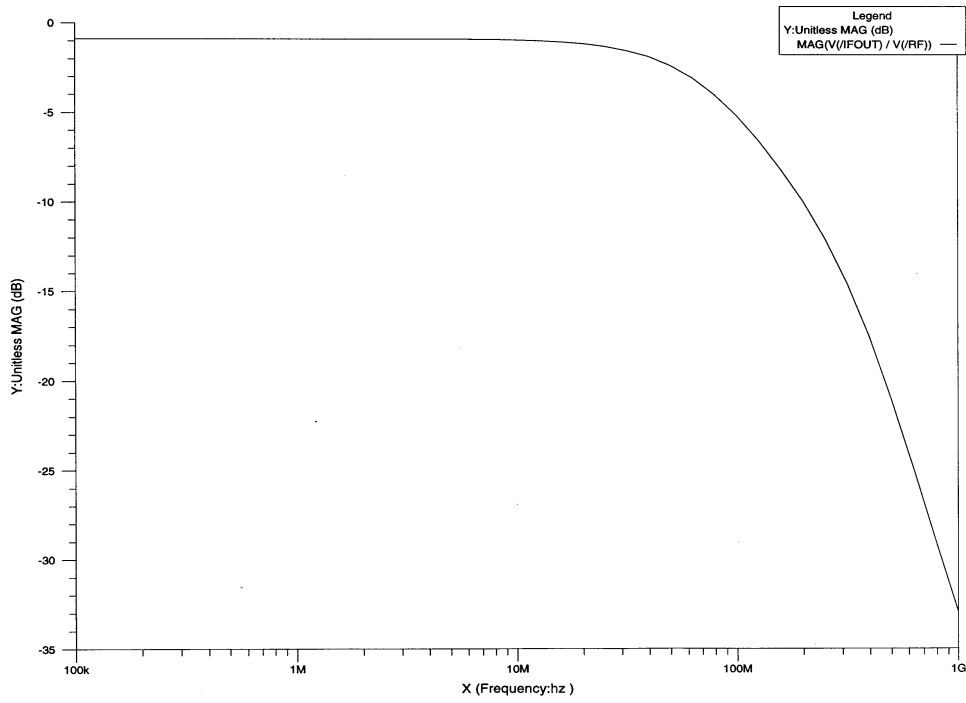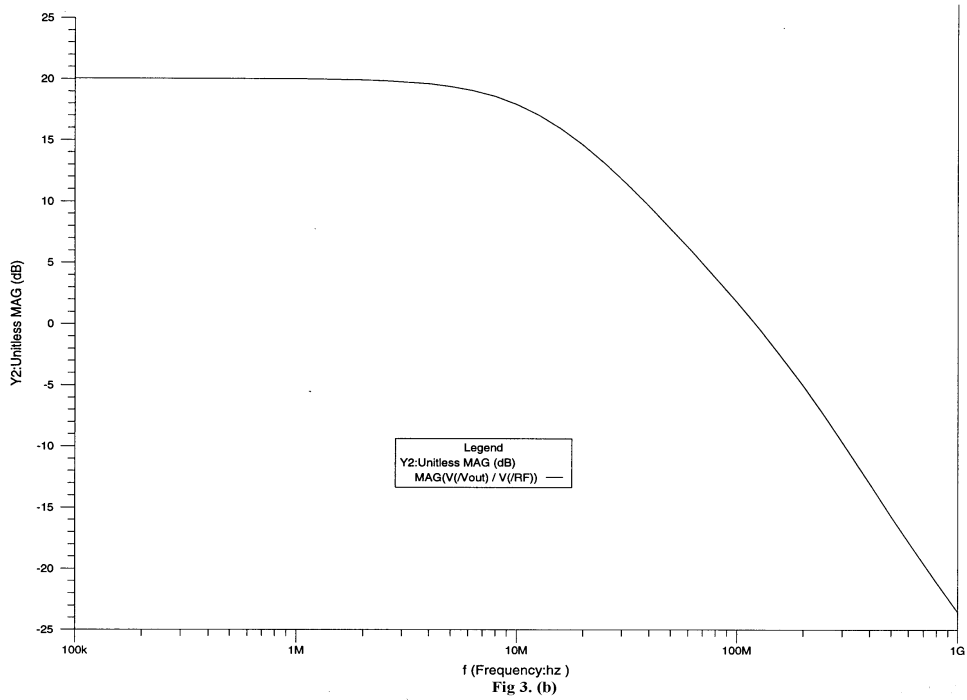

Fig 2. (b)

Simulation Curve for CMOS

The frequency response (dB v/s frequency) of BJT and CMOS technology is shown by Fig 3. (a) and Fig 3. (b). The layout of the BJT and CMOS is compared for current and the area.
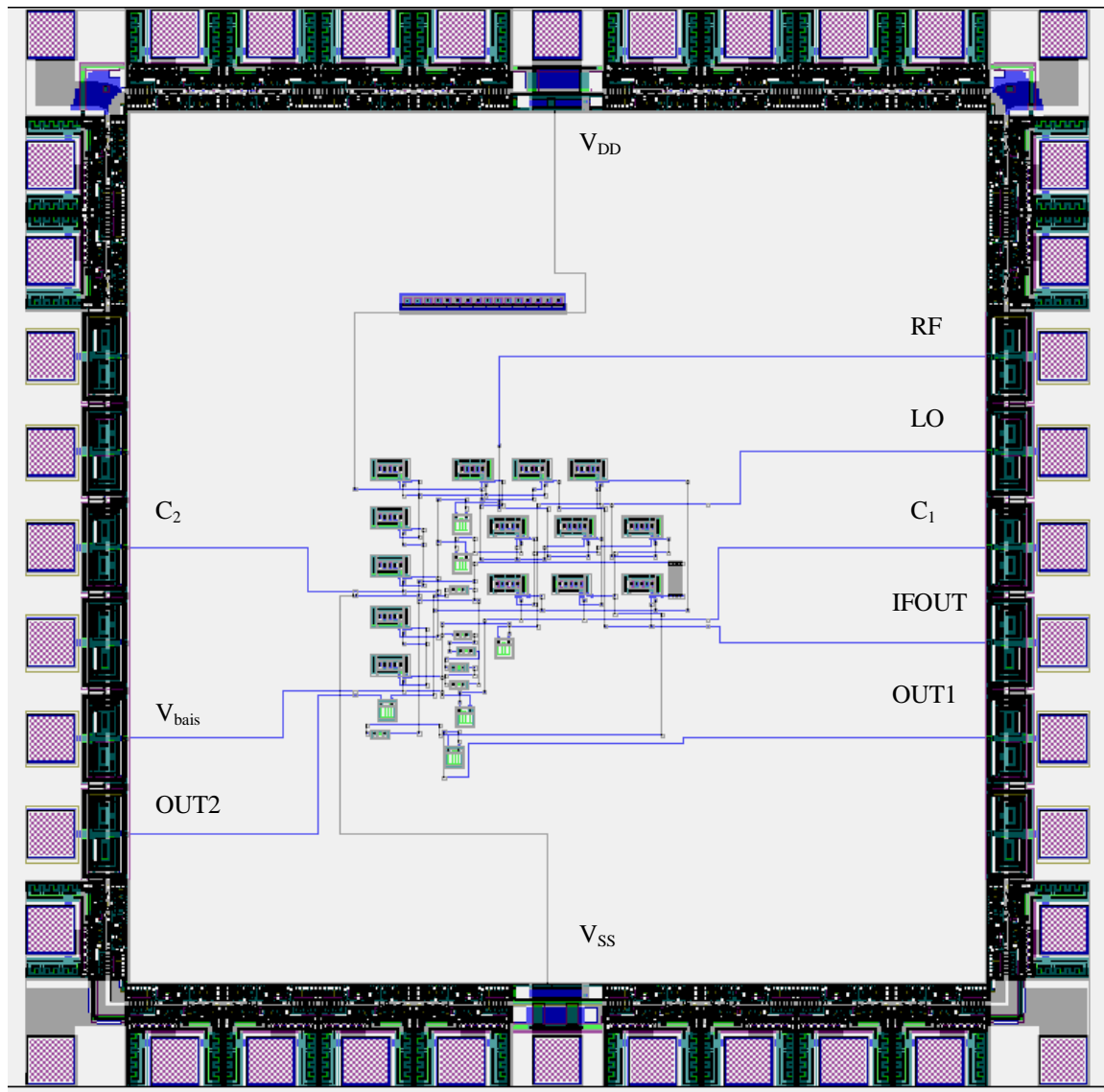
Fig 3. (a)

Analog Trace

Fig 3. (b)

Fig. 4. (a)

The Fig 4. (a) Shows the layout for BJT technology, which was taped out for fabrication. All the ports were brought to their corresponding padframes and the design was fabricated in 2-micron technology. The Fig 4. (b) Shows a comparison between the areas of CMOS and BJT, although the current for BJT was 2 ma and the current for CMOS was 56 μa. The area for BJT is 145710 sq.microns for the current of 2 ma whereas the area of CMOS is 50500 sq.microns for 56 μa.
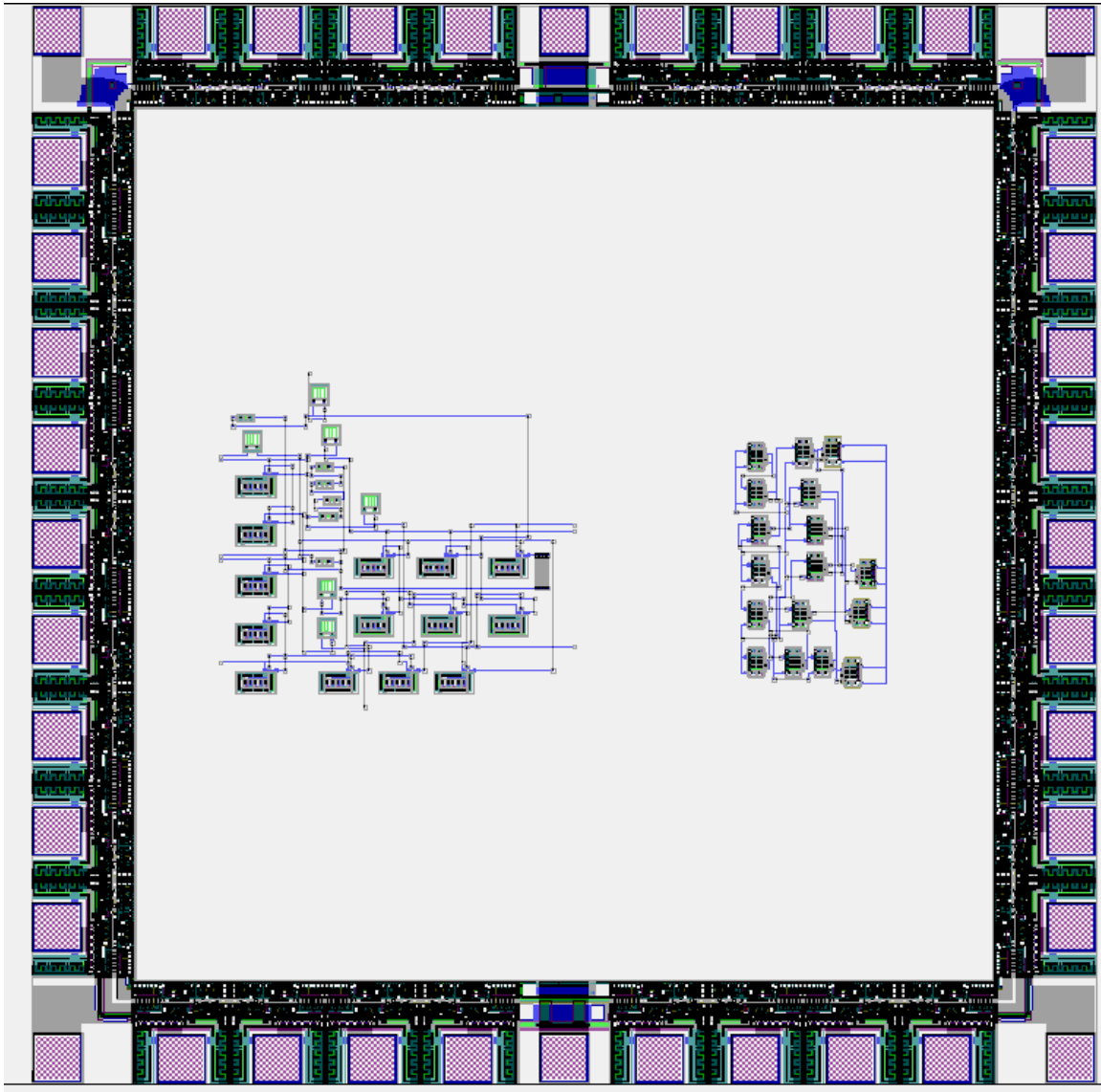
Fig. 4. (b)

IV. Test results for BJT

The chip was tested on its return from the foundry. The supply voltage of Vdd – 5 V was given and the capacitors of 470µF were used externally. The RF input of 50 mv at 10 MHz was applied at the RF port via a coupling capacitor of 470 µF. The LO input of 50 mv @ 1 MHz was applied at the LO port via a external capacitor of 470 µF. All the

remaining ports were AC grounded to avoid the mismatch in the circuit and to block the single ended input from propagating to the other input. The resultant output seen at the IFOUT port shows that the mixer is a downconverter as predicted.
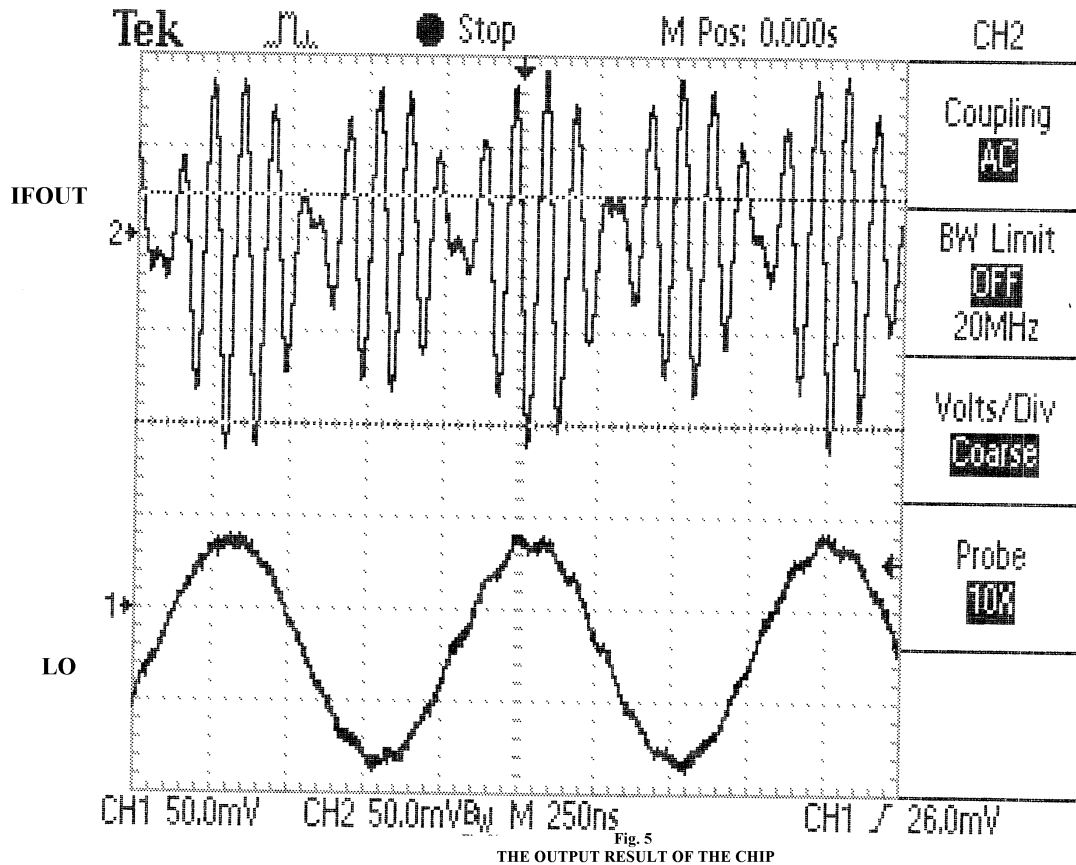

Fig. 5
THE OUTPUT RESULT OF THE CHIP

Fig. 5 shows the waveforms of IFOUT port and the LO port. We can conclude that the output changes every time when the input LO goes to zero thereby indicating perfect modulation.

V. Conclusion

A four quadrant Gilbert Cell mixer was designed and fabricated in BJT technology. The circuit approach is based on doubly balanced four quadrant Gilbert Cell topology. Simulations were done for both CMOS and BJT technology, but only the design of BJT technology was fabricated into a chip and tested for the results. Though it should be noted that the performance of a BJT Gilbert Cell mixer implemented is lower than the measured performance of this mixer because of the inability to generate ideal fully differential RF and LO signals on chip and poorer on-chip matching.

VI. References

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